Chapter 6

Reliability Analysis

6.1 Introduction

Reliability is the probability that a device will perform its intended working for a specified period of time under normal operation. Reliability function is the ration of N(t1) is the number of healthy and working devices at the moment t1 and N(t0) is the number of healthy devices at the moment of t0. Another definition of R(t) is the probability of a device working overtime interval of [0, t]. The limitations for R(t) is $R(0) = 1$ and $R(\infty) = 0$.

Markov evaluation approach is nowadays well attempted and used for calculating and comparing the reliability of different system. Markov evaluation approach is applied to calculate the reliability by making the Markov chain and by considering the operation of system in different states from healthy operation to the failure of whole system.

6.2 Markov evaluation approach

Markov chain diagram of the multilevel inverter is presented in Fig. 6.1. When a fault occurs in one of the switches, the entire system will be failed. So, two states are defined as state 1 in which all components are healthy and system is operating in normal mode and state 2 in which a component fails and the whole system is failed. Reliability calculations for cascaded H-bridge 7-level multilevel inverter are as given in equation (1) to (4). Where λ_{Sw} and λ_D are failure rates of switches and diodes.

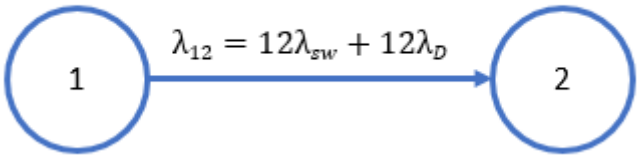

Figure 6.1: Markov chain of cascaded H-bridge 7-level inverter

Markov Transition Chain,

$$\lambda_{12} = 12\lambda_{sw} + 12\lambda_D \quad (1)$$

Initial condition,

$$P(0) = [1\ 0] \quad (2)$$

Stochastic matrix,

$$P = \begin{bmatrix} 1 - (12\lambda_{sw} + 12\lambda_D) & (12\lambda_{sw} + 12\lambda_D) \\ 0 & 1 \end{bmatrix} \quad (3)$$

Reliability,

$$R(t) = P1(t) = e^{-(12\lambda_{sw} + 12\lambda_D)t} \quad (4)$$

Markov chain diagram for the proposed structure is shown in Fig. 6.2. In state 1, all components are healthy and the circuit is operating in 7-level mode. If any failure occurs in a component and if all the related relays operate accurately, circuit will move to second state with transition given in equation (5). Where P_R is the probability that the fault management mechanism. If relays do not operate accurately then system will fail and it will transmitted to state 4 with Markov chain transition given in equation (6). In state 2, the inverter is operating with two modules. In this state, if a failure occurs in a component and the fault management mechanism operates accurately then the whole system will lead to state 3 with Markov chain transition given in equation (7). If the fault management mechanism does not work accurately the whole system will be failed and transmitted to state 4 with Markov chain transition given in equation (8). In state 3, the system is working with 1-module and the fault management system work properly. Now, after the next failure occurred the system will be failed by the Markov chain transition given in equation (9).

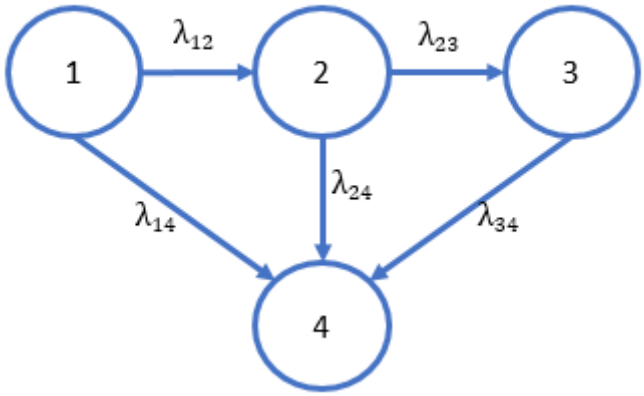

Figure 6.2 Markov chain of proposed FT cascaded H-bridge 7-level inverter

Markov Transition Chain,

$$\lambda_{12} = (12\lambda_{sw} + 12\lambda_D)\, P_r \quad (5)$$

$$\lambda_{14} = (12\lambda_{sw} + 12\lambda_D)\, (1 - P_r) \quad (6)$$

$\lambda_{23} = (8\lambda_{sw} + 8\lambda_D)\, P_r$ (7)

$\lambda_{24} = (8\lambda_{sw} + 8\lambda_D)\, (1 - P_r)$ (8)

$\lambda_{34} = (4\lambda_{sw} + 4\lambda_D)$ (9)

The Initial condition is given as

$P(0) = [1\ 0\ 0\ 0]$ (10)

Stochastic matrix (P) is expressed as,

$$P = \begin{bmatrix} 1-(\lambda_{12}+\lambda_{14}) & \lambda_{12} & 0 & \lambda_{14} \\ 0 & 1-(\lambda_{23}+\lambda_{24}) & \lambda_{23} & \lambda_{24} \\ 0 & 0 & 1-\lambda_{34} & \lambda_{34} \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (11)$$

The reliability of the system based on all three states are given as,

$R(t) = \sum_{i=1}^{3} Pi(t) = P1(t) + P2(t) + P3(t)$ (12)

Probability of each state is expressed as,

$$P1(t) = e^{-(\lambda 12 + \lambda 14)t} \quad (13)$$

$$P2(t) = \frac{\lambda 12}{\lambda 23+\lambda 24-\lambda 12-\lambda 14}\left[e^{-(\lambda 12+\lambda 14)t} - e^{-(\lambda 23+\lambda 24)t}\right] \quad (14)$$

$$P3(t) = \frac{\lambda 12\lambda 23}{(\lambda 12+\lambda 14-\lambda 34)(\lambda 23+\lambda 24-\lambda 34)}\left[e^{-(\lambda 34)t}\right] + \frac{\lambda 12\lambda 23}{(\lambda 34-\lambda 12-\lambda 14)(\lambda 23+\lambda 24-\lambda 12-\lambda 14)}\left[e^{-(\lambda 12+\lambda 14)t}\right] + \frac{\lambda 12\lambda 23}{(\lambda 34-\lambda 23-\lambda 24)(\lambda 12+\lambda 14-\lambda 23-\lambda 24)}\left[e^{-(\lambda 23+\lambda 24)t}\right] \quad (15)$$

Failure rates of power electronic components are calculated as,

$\lambda_{component} = \lambda_b \sum_{i=1}^{n} \pi_i$, Failure/$10^6$h (16)

Where, n is the number of factors affecting the component failure rate and λ_b is the basic failure rate of component which is related to the component quality and its performance at a given temperature. To evaluate the influence of temperature, it is necessary to calculate the power loss of component.

The effective factor of switches and diodes are given as,

$\lambda_{sw} = \lambda_b\, \pi_T\, \pi_A\, \pi_Q\, \pi_E$ (17)

$\lambda_D = \lambda_b\, \pi_T\, \pi_S\, \pi_C\, \pi_Q\, \pi_E$ (18)

The temperature factor of the switches and diodes are given by following equations,

$\pi_T = \exp\left[-1925\left(\frac{1}{\mathrm{Tj}+273} - \frac{1}{298}\right)\right]$ (19)

$$\pi_D = \exp\left[-3091\left(\frac{1}{\mathrm{Tj}+273}-\frac{1}{298}\right)\right] \quad (20)$$

The junction temperature is calculated by using following equations,

$$Tj = Tc + \theta_{\mathrm{jc}}\,\mathrm{P}_D \quad (21)$$

$$Tc = Ta + \theta_{\mathrm{ja}}\,\mathrm{P}_D \quad (22)$$

The power loss consists of two parts. One is conduction loss (P_D) and switching loss (P_{Dsw}) that are calculated through equations (23) and (24). For calculation the parameters are considered form datasheets of switch and diode which are used in hardware. The details of other factors are given in Table 6.1.

$$P_D = \frac{1}{\mathrm{T}}\left[\int_o^T R_d\, {i_s}^2(t) + \mathrm{V}_f\, \mathrm{i}_D(\mathrm{t})\right] \quad (23)$$

$$P_{Dsw} = \frac{Vs*fs}{2} * \left[\mathrm{t}_{on} + \mathrm{t}_{off}\right] * \mathrm{I}_{on} \quad (24)$$

Quality factor of component, π_Q	1
Contact construction factor, π_C	2
Effect of the environment, π_E	1
Application factor, π_A	8
Electrical stress factor of a diode, $\pi_S = \mathrm{V}_s^{2.43}$	0.02834
Failure rate of switch, $\lambda_{b,sw}$	0.06
Failure rate of diode, $\lambda_{b,D}$	0.0038

Table 6.1: Different Factors details

The calculated values of junction temperature, temperature factor and effective factor are calculated using equation (17) – (22) and above data are given in Table 6.2.

Junction temperature	T_j, SW	79.41
	T_j, D	61.39
Temperature factor	π_T, SW	2.711
	π_T, D	3.091
Effective factors	λ_{sw}	1.3012
	λ_D	0.00066

Table 6.2: Calculated values of junction temperature, temperature factor & effective factor

Calculated values of failure rates of Markov transition chain from equation (5) – (9) are given in Table 6.3.

Failure rates of each Markov transition chain	λ_{12}	14.060
	λ_{14}	1.5622
	λ_{23}	9.3733
	λ_{24}	1.0414
	λ_{34}	5.2074

Table 6.3: calculated values of failure rates

Probability of each state from equation (13) – (15) are given as,

$$P1(t) = e^{-15.622t} \quad (25)$$

$$P2(t) = 2.70\,[e^{-10.4147t} - e^{-15.622t}] \quad (26)$$

$$P3(t) = 2.430\,[e^{-5.2074t}] + 2.4275\,[e^{-15.6222t}] - 4.8595\,[e^{-10.4147t}] \quad (27)$$

From equation (12), the reliability of fault-tolerant cascaded H-bridge 7-level multilevel inverter is given as,

$$R(t) = 0.7275\,e^{-15.622t} - 2.1595\,e^{-10.4147t} + 2.430\,e^{-5.2074t} \quad (28)$$

From equation (4), the reliability of cascaded H-bridge 7-level multilevel inverter is given as,

$$R(t) = e^{-15.6223t} \quad (29)$$

By plotting the graph of the equation (28) and (29) as given Fig. 3, it is found that the reliability of fault-tolerant cascaded H-bridge 7-level multilevel inverter is more as compare to the cascaded H-bridge 7-level multilevel inverter.

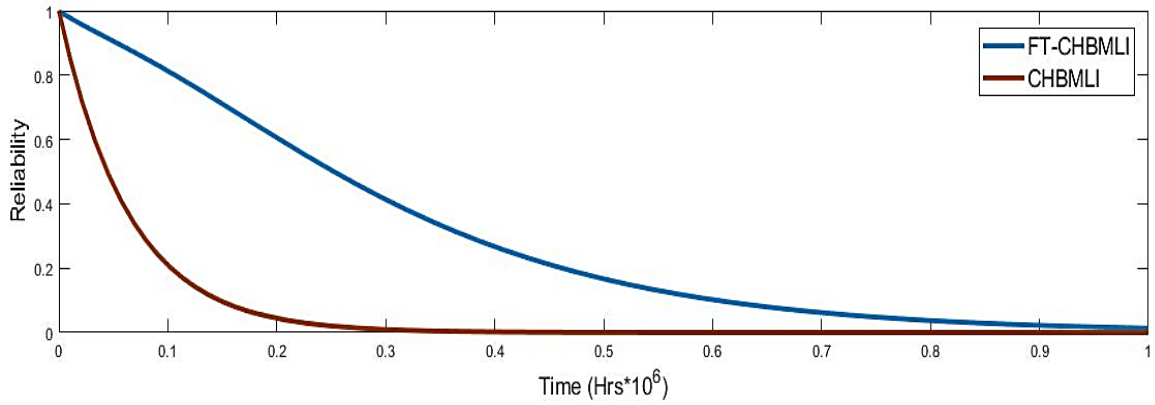

Figure 6.3: Comparison of reliability of FT-CHBMLI and CHBMLI

Conclusion

This thesis presents a fault-tolerant structure designed for a 7-level Cascaded H-Bridge Multi-Level Inverter (CHBMLI) consisting of 3 modules. The primary objective of this structure is to ensure the "continuous operation" of the inverter even when one or two modules experience faults. This objective is achieved by incorporating an additional set of 9 single-pole single-throw (SPST) and 9 single-pole double-throw (SPDT) relays to isolate the voltage source(s) of the faulty module(s) and bypass the faulty module(s) to maintain the functionality of the remaining healthy system.

A hardware model is developed and rigorously tested under various fault conditions. The simulation results align closely with the hardware results, demonstrating the effectiveness of the proposed fault-tolerant structure for CHBMLI. This approach significantly enhances system reliability by preventing a complete system breakdown as long as at least one module remains operational. The testing shows that the Fault-Tolerant CHBMLI (FT-CHBMLI) offers superior reliability when compared to the conventional CHBMLI.