Bibliography

Journals

[1] Mariusz Malinowski, K. Gopakumar, Jose Rodriguez, and Marcelo A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[2] Samir Kouro, Mariusz Malinowski, K. Gopakumar, Josep Pou, Leopoldo G. Franquelo, BinWu, Jose Rodriguez, Marcelo A. Pérez, and Jose I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] Wenping Zhang, Dehong Xu, Prasad N. Enjeti, Haijin Li, Joshua T. Hawke, and Harish S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[4] Anjali Anand, Nithin Raj, Saly George, and Jagadanand G., "Open switch fault detection in cascaded H-bridge multilevel inverter using normalised mean voltages," in *Proc. IEEE 6th International Conference on Power Systems (ICPS 2016)*, Apr. 2016, pp. 764–775.

[5] Seok-Min Kim, June-Seok Lee, and Kyo-Beum Lee, "A modified level-shifted PWM strategy for fault-tolerant cascaded multilevel inverters with improved power distribution," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7264-7274, Nov. 2016.

[6] Hossein Khoun Jahan, Farhad Panahandeh, Mehdi Abapour, and Sajjad Tohidi, "Reconfigurable multilevel inverter with fault-tolerant ability," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7880-7893, Sep. 2018.

[7] Mohammad Mehdi Haji-Esmaeili, Mersad Naseri, Hossein Khoun-Jahan, and Mehdi Abapour, "Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation," *IET Power Electronics*, vol. 10, iss. 1, pp. 59-70, Jan. 2017.

[8] Huai Wang, Marco Liserre, Frede Blaabjerg, Peter de Place Rimmen, John B. Jacobsen, Thorkild Kvisgaard, and Jorn Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97-114, Mar. 2014.

[9] Haitham Abu-Rub, Joachim Holtz, Jose Rodriguez, and Ge Baoming, "Medium-voltage multilevel converters - state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[10] Marcelo A. Perez, Steffen Bernet, Jose Rodriguez, Samir Kouro, and Ricardo Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4-17, Jan. 2015.

[11] Suman Debnath, Jiangchao Qin, Behrooz Bahrani, Maryam Saeedifard, and Peter Barbosa, "Operation, control, and applications of the modular multilevel converter: a review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37-53, Jan. 2015.

[12] Nithin Raj, Saly George, and Jagadanand G., "Open transistor fault detection in asymmetric multilevel inverter," in *Proc. IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES)*, Feb. 2016, pp. 1-5.

[13] Nithin Raj, Anjali Anand, Jagadanand G., and Saly George, "Output voltage modeling of cascaded H-bridge multilevel inverters under open-transistor fault," in *Proc. IEEE Industrial Electronics and Applications Conference (IEACon)*, Nov. 2016, pp. 7-11.

[14] Nithin Raj, Anjali Anand, Ahammed Riyas, Jagadanand G, and Saly George, "A novel open-transistor fault detection method in symmetric cascaded H-bridge multilevel inverter," in *Proc. IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec. 2016, pp. 1-6.

[15] Parvin Moamaei, Hamid Mahmoudi, and Reza Ahmadi, "Fault-tolerant operation of cascaded H-bridge inverters using one redundant cell," in *Proc. IEEE Power and Energy Conference at Illinois (PECI)*, 2015.

DrillBit

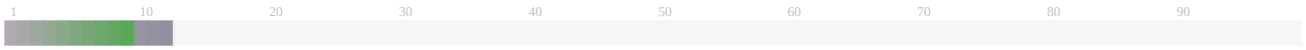
The Report is Generated by DrillBit Plagiarism Detection Software

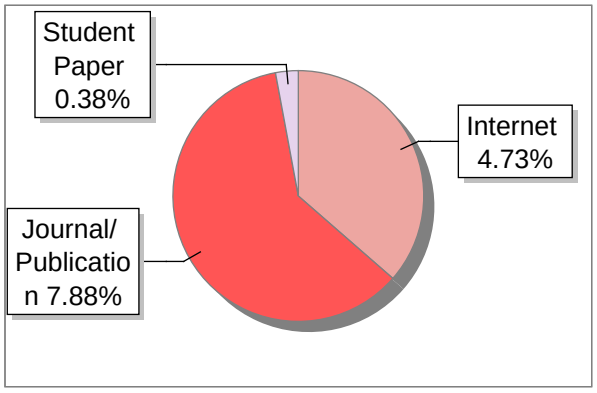
Submission Information

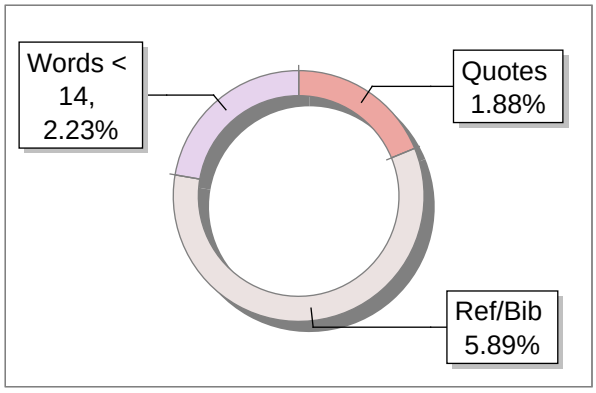
Author Name	MOnika Patel
Title	Thesis
Paper/Submission ID	1192178
Submitted by	librarian@atmiyauni.ac.in
Submission Date	2023-12-10 22:21:02
Total Pages	78
Document type	Thesis

Result Information

Similarity **13 %**







Exclude Information

Quotes	Not Excluded
References/Bibliography	Excluded
Sources: Less than 14 Words %	Excluded
Excluded Source	**2 %**
Excluded Phrases	Not Excluded

Database Selection

Language	English
Student Papers	Yes
Journals & publishers	Yes
Internet or Web	Yes
Institution Repository	Yes

A Unique QR Code use to View/Download/Share Pdf File

DrillBit

DrillBit Similarity Report

13	25	B
SIMILARITY %	MATCHED SOURCES	GRADE

A-Satisfactory (0-10%)
B-Upgrade (11-40%)
C-Poor (41-60%)
D-Unacceptable (61-100%)

LOCATION	MATCHED DOMAIN	%	SOURCE TYPE
1	Thesis Submitted to Shodhganga Repository	3	Publication
2	Fault-Tolerant and Reliable Structure for Cascaded Quasi-Z Source DC-D by Haji-Esmaeili-216	1	Publication
3	Reconfigurable Multilevel Inverter with Fault Tolerant Ability, by Hossein, Khoun Jaha- 2017	1	Publication
4	moam.info	<1	Internet Data
5	mdpi.com	1	Internet Data
6	High-Frequency Link A Solution for Using Only One DC Source in Asymmetric Casca by Pereda-2011	1	Publication
7	ccc.msubaroda.ac.in	<1	Internet Data
8	ccc.msubaroda.ac.in	<1	Internet Data
9	ccc.msubaroda.ac.in	<1	Internet Data
10	ccc.msubaroda.ac.in	<1	Internet Data
11	ccc.msubaroda.ac.in	<1	Internet Data
13	Thesis Submitted to Shodhganga Repository	<1	Publication
14	ccc.msubaroda.ac.in	<1	Internet Data

15	ccc.msubaroda.ac.in	<1	Internet Data
16	A NEW HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR MULTI By 15BH1D4312 - 2018, JNTUH	<1	Student Paper
17	Thesis Submitted to Shodhganga, shodhganga.inflibnet.ac.in	<1	Publication
19	A Switched-Capacitor Sub-Module for Modular Multilevel HVDC Converters by Elserougi-2015	<1	Publication
20	Thesis Submitted to Shodhganga Repository	<1	Publication
21	moam.info	<1	Internet Data
23	IEEE 2018 IEEE 5th International Congress on Information Science an, by Hmidet, Ali Hasnao- 2018	<1	Publication
24	Thesis submitted to shodhganga - shodhganga.inflibnet.ac.in	<1	Publication
25	qdoc.tips	<1	Internet Data
27	docplayer.net	<1	Internet Data
28	hdtv.appcreatar.com	<1	Internet Data
29	moam.info	<1	Internet Data

EXCLUDED SOURCES

12	Institute of Electrical and Electronics Engineers Article	<1	Publication
18	Thesis Submitted to Shodhganga Repository	<1	Publication
22	New Analytical Model for RealTime Junction Temperature by Merouane Ouhab - ieeeexplore.org	<1	Publication
26	IEEE 2015 International Conference on Electrical, Electronics, Signa by	<1	Publication

32	IEEE 2018 IEEE International Power Electronics and Application Conf, by Qiao, Yang Zhang, - 2018	<1	Publication
33	www.inderscience.com	<1	Internet Data
46	www.ijetae.com	<1	Publication

Publications

International Journal

[1] Patel, Monika D., and Pandya, D. J., (2023). Fault-Tolerant Structure for Cascaded H-bridge Multilevel Inverter for Double Module Faults. *GIS-Zeitschrift fur Geoinformatik Journal*, 2022. ISSN 1869-9391.
Indexing: **Scopus**

International Conference

[2] Patel, M.D., Pandya, D.J., Raval, D.Y., and Yagnik, N.Y. (2019). Fault-Tolerant Structure for Cascaded H-bridge Multilevel Inverter using Relays. *8th International Conference on Computation of Power, Energy, Information and Communication*, ICCPEIC 2019, 2019, pp. 8–13, 9082384.
Indexing: **Scopus**

Fault-Tolerant Structure for Cascaded H-bridge Multilevel Inverter using Relays

Monika D. Patel[1], D. J. Pandya, Dhaval Y. Raval and Niral Yagnesh Yagnik
Department of Electrical Engineering
Atmiya Institute of Technology & Science
Rajkot, India
monikapatel1985@gmail.com

***Abstract*—Cascaded H-bridge multilevel inverter (CHBMLI) is the most popular topology for high power industrial applications. There are total 4*m* number of power electronic switches in a CHBMLI having *m* numbers of modules (*m*>1). Because of higher number of switches; the possibility of faults in switches is more. A fault-tolerant structure is proposed for CHBMLI having 3 modules. If any 1 out of 3 modules gets faulty; the remaining 2 healthy modules will continue delivering output voltage with the same amplitude and the same voltage level as in case of normal operation having all the 3 modules are healthy. In this way, the proposed fault-tolerant structure of CHBMLI improves the system reliability by preventing the breakdown of the whole system even if 1 out of 3 modules gets faulty.**

Keywords—fault detection, fault tolerant, cascaded H-bridge, multilevel inverter, LS-PWM

Introduction

With widespread application of multilevel inverters in various industrial systems; there has been a rising interest in system reliability analysis and fault-tolerant capabilities [1]. The three most popular and widely used families of multilevel inverters in industry are neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB). Among these; cascaded H-bridge multilevel inverter is extensively used in high power industrial applications because of its modularity feature [2]–[3].

Since the multilevel inverters use a large number of power electronic switches; the probability of switch faults is more. Power electronic switches are the most vulnerable components in a multilevel inverter as compared to other components. Open switch and short circuit are the most frequent faults in a power electronic switch [4]. Due to a large number of power electronic switches; detection of type and location of a fault can be complicated in principle. Hence, the detection of probable faults and the operation under faulty conditions are of paramount importance. Since most of the multilevel inverters do not exhibit redundancy; any fault that occurs to components or subsystems will result in interruption of the operation.

In order to improve reliability of an inverter; some methods include additional hardware and reconfiguration of the structure, which allows operation of the inverter under fault condition. These methods also modify the software, principally the modulation strategy [5]. For most of fault-tolerant solutions; the physical fault isolation is the first step, especially in case of short circuit fault. The fault-isolation unit forces damaged switches or poles to be electrically isolated from the system, which can eliminate its influence over the remaining healthy part of the system. After the fault isolation; fault reconfiguration is activated. This process relies on hardware redundancy design and corresponding fault-tolerant control [1]. The availability of powerful microprocessors made it possible to develop intelligent methods to recognize faults quickly; using a reduced number of sensors by analyzing the inverter output parameters *viz.* voltage and current [5]. Basically, input voltage and output voltage or input current and output current characteristics of an inverter under normal condition and fault condition are different from each another. These electrical parameters are sensed and compared with reference performance metrics to determine whether a fault has happened and identify faulty component and type of fault [6]

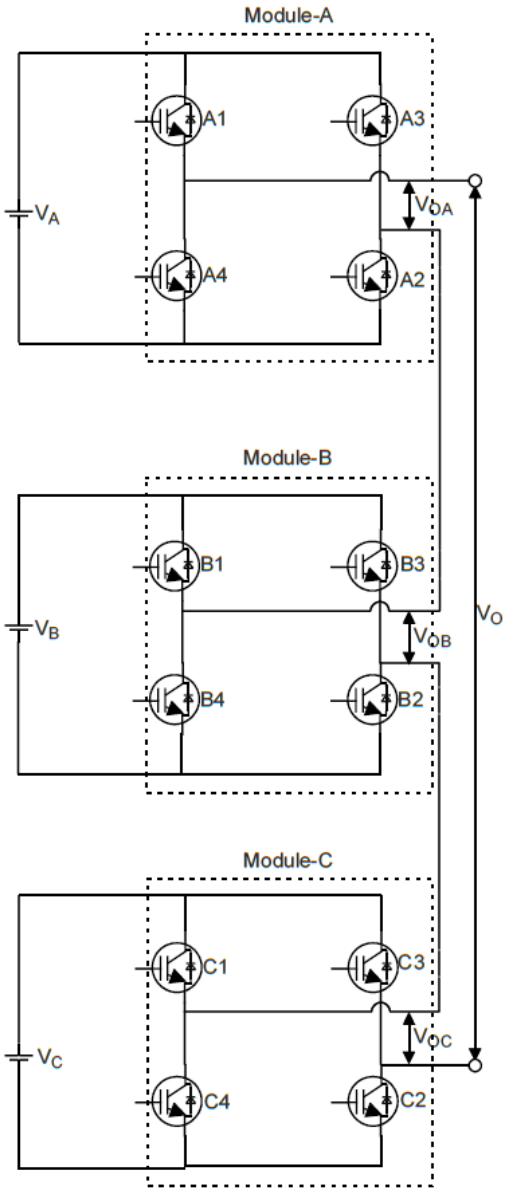


Fig. 1. Classical cascaded H-bridge multilevel inverter

Multilevel inverters and especially cascaded H-bridge multilevel inverters can tolerate open switch and short circuit faults after bypassing faulty modules and reconfiguring the switching pattern to operate rest of the healthy modules [7].

978-1-7281-0837-7/19/$31.00

A fault-tolerant structure is proposed for CHBMLI having 3 modules. In which, if any 1 module gets faulty; the remaining 2 healthy modules will continue delivering output voltage with the same amplitude and the same voltage level as in case of normal operation having all the 3 modules are healthy [8]–[9]. The faulty module is bypassed using ordinary relays. Continuity of operation is the key feature of the proposed fault-tolerant structure.

I. Proposed Fault Tolerant Structure for CHBMLI

A. Cascaded H-Bridge multilevel inverter

Cascaded H-bridge multilevel inverter consists of series connected H-bridges. A CHBMLI with N number of similar DC voltage sources gives ($2N$+1) levels at the output phase voltage.

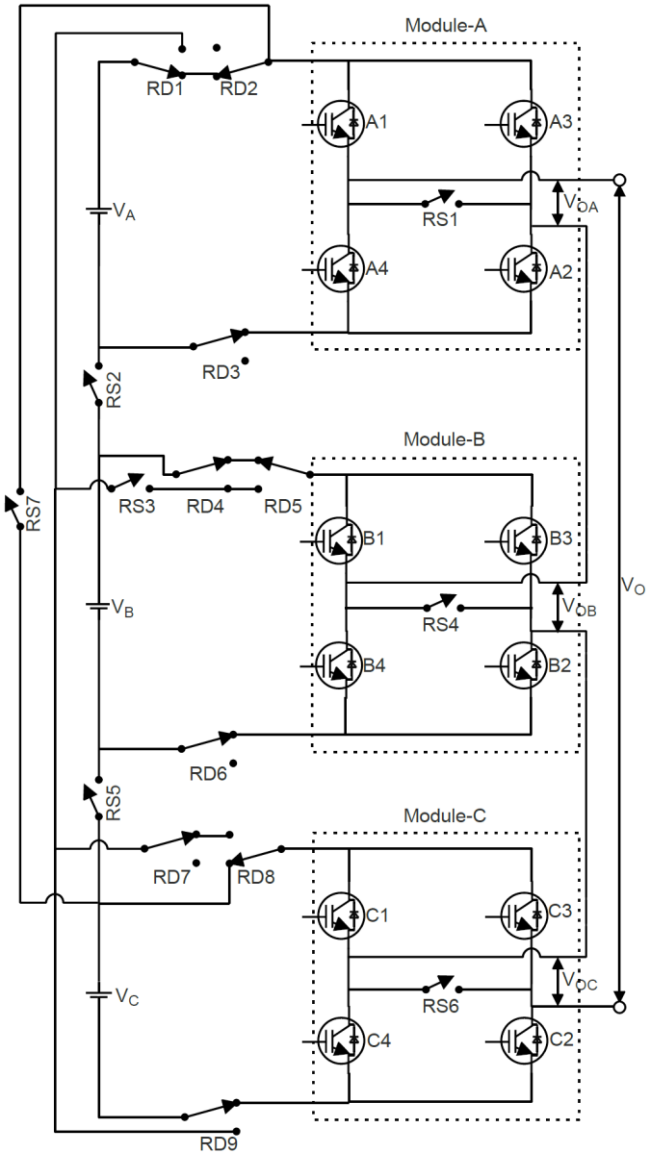


Fig. 2. Proposed fault-tolerant structure for CHBMLI

Fig. 1 shows a classical single phase 7-level cascaded H-bridge multilevel inverter having 3 modules *viz.* Module-A, Module-B and Module-C. To generate 7-level output voltage; CHBMLI uses 3 separate voltage sources having equal magnitude *i.e.* $V_A = V_B = V_C = V_{dc}$. In Fig. 1; A1-A4, B1-B4 and C1-C4 are IGBTs forming 3 H-bridges. V_{OA}, V_{OB} and V_{OC} are instantaneous output voltages of individual modules. V_O represents total instantaneous output voltage of CHBMLI.

B. Proposed fault-tolerant structure for CHBMLI

Fig. 2 represents proposed fault-tolerant structure for a 7-level CHBMLI. Additional 16 relays are used to divert current path during faulty operation. In Fig. 2; RS1-RS7 are single pole single throw (SPST) relays and RD1-RD9 are single pole double throw (SPDT) relays. When any 1 module gets faulty; operation of CHBMLI remains continue by two actions: (i) isolation of faulty module and (ii) connecting the source of faulty module in series with one of the sources of healthy modules. Different modes of operation for proposed fault-tolerant CHBMLI are shown in Table I.

TABLE I. Mode of Operation

Module-A	Module-B	Module-C	Operation
H	H	H	Mode-0
F	H	H	Mode-1
H	**F**	H	Mode-2
H	H	**F**	Mode-3

In TABLE I; H indicates healthy condition of module and F indicates faulty condition of module. Mode-0 is normal condition of CHBMLI. Mode-1, Mode-2 and Mode-3 are faulty conditions of CHBMLI.

TABLE II. Relay Operation

Relay	Mode-0	Mode-1	Mode-2	Mode-3
RS1	0	**1**	0	0
RS2	0	**1**	0	0
RS3	0	**1**	**1**	0
RS4	0	0	**1**	0
RS5	0	0	**1**	0
RS6	0	0	0	**1**
RS7	0	0	0	**1**
RD1	0	**1**	0	**1**
RD2	0	0	0	0
RD3	0	**1**	0	0
RD4	0	0	**1**	0
RD5	0	**1**	0	0
RD6	0	0	**1**	0
RD7	0	0	0	**1**
RD8	0	0	**1**	**1**
RD9	0	0	0	**1**

TABLE II shows relay condition in different mode of operation. 0 indicates rest or unchanged state and 1 indicates operated or changed state of respective relay. In Mode-0; all the relays remain in rest state. When any 1 module gets faulty; 6 out of 16 relays are operated to ensure isolation of faulty module and utilization of the source of faulty module. CHBMLI normally operating in symmetrical configuration starts operating in asymmetrical configuration during faulty condition in order to generate 7-level output voltage with the same voltage amplitude.

978-1-7281-0837-7/19/$31.00 ©2019 IEEE

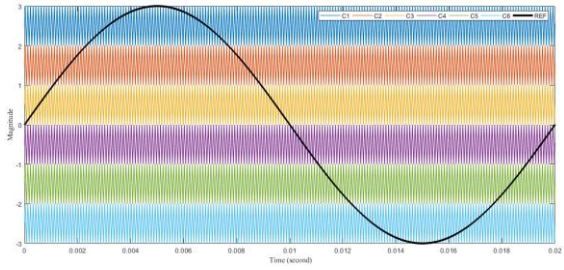


Fig. 3. LS-PWM

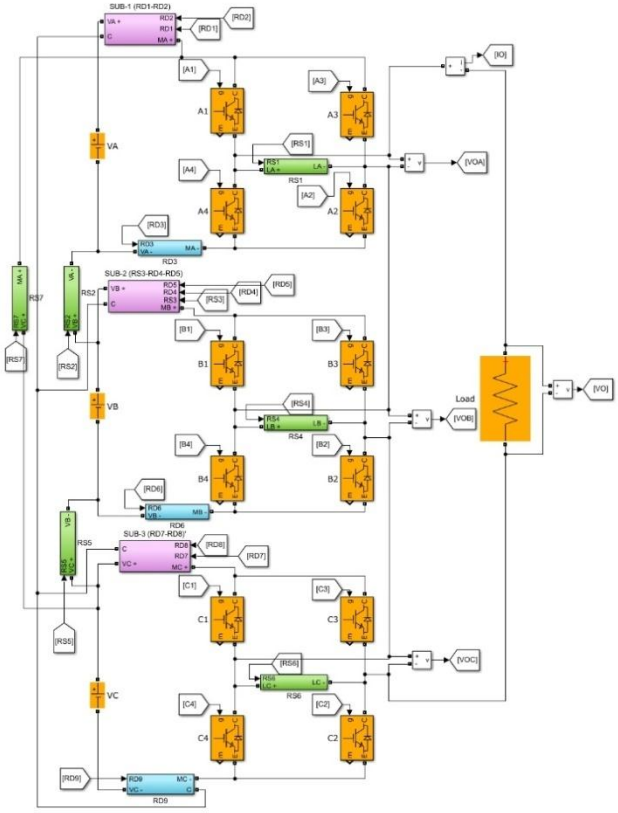


Fig. 4. Simulink model of proposed fault-tolerant structure

C. Sector-based switching

As CHBMLI changes its operational nature from symmetrical to asymmetrical during faulty condition; sector-based PWM has been utilized to change modulation strategy of CHBMLI. Phase disposed LS-PWM using 6 carrier (triangular, C1-C6) and 1 reference (sinusoidal, Ref) as shown in Fig. 3 has been utilized to form 8 sectors which indeed represents 7 output voltage levels [10]. Sector segregation as Ref travels through C1-C6 has been described in TABLE III.

TABLE III. SECTOR SEGREGATION

Sr.	Condition	Sector
1	*Ref > C1*	S1
2	*C1 ≥ Ref > C2*	S2
3	*C2 ≥ Ref > C3*	S3
4	*C3 ≥ Ref > 0*	S4
5	*0 ≥ Ref > C4*	S5
6	*C4 ≥ Ref > C5*	S6
7	*C5 ≥ Ref > C6*	S7
8	*Ref ≤ C6*	S8

II. SIMULATION AND RESULTS

Proposed fault-tolerant CHBMLI has been validated by carrying out simulation in MATLAB Simulink as shown in Fig. 4. In Fig. 4; SUB-1, SUB-2 and SUB-3 are subsystems to form logical combination of relays. SUB-1 consists of RD1 and RD2, SUB-2 consists of RS3, RD4 and RD5, SUB-3 consists of RD7 and RD8. Interconnections between the relays of the respective subsystems are shown in Fig. 2 itself.

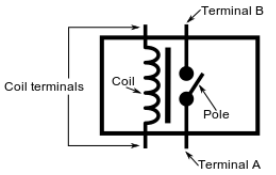


Fig. 5. Typical SPST relay

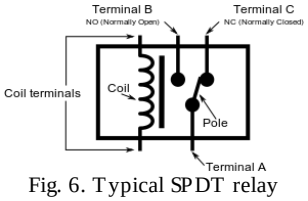


Fig. 6. Typical SPDT relay

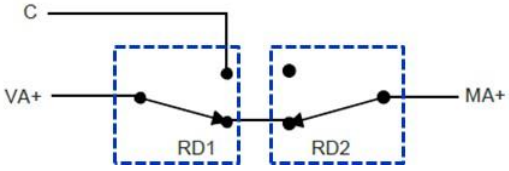


Fig. 7. Logical Switch (SUB-1)

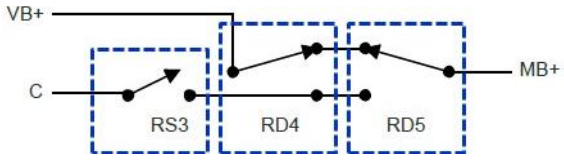


Fig. 8. Logical Switch (SUB-2)

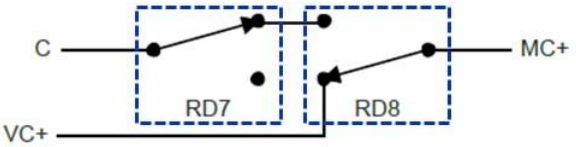


Fig. 9. Logical Switch (SUB-3)

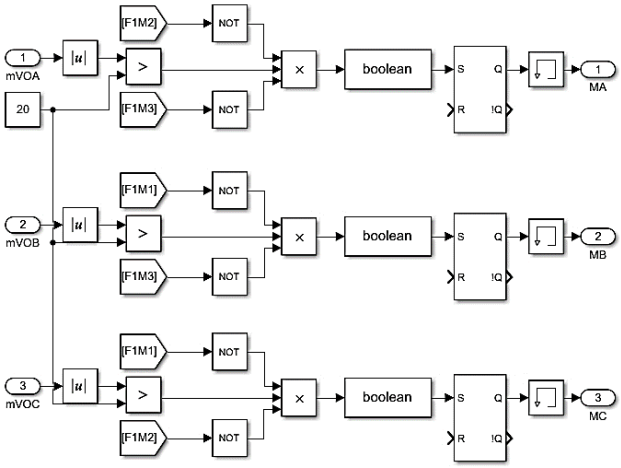


Fig. 10. Fault detection logic

Fig. 5 and Fig. 6 show typical diagrams of SPST and SPDT relays respectively which have been utilized to form logical switches represented as SUB-1, SUB-2 and SUB-3 as shown in Fig. 7, Fig. 8 and Fig. 9 respectively. These logical switches ensure isolation of faulty module and utilization of source of faulty module. Different connection can be possible within this logical switches as per mode of operation. As shown in Fig. 7; SUB-1 is connected to Module-A, C represents common rail of fault-tolerant

CHBMLI, VA+ represents positive terminal of V_A and MA+ represents positive terminal of Module-A. Similar notations are used in Fig. 8 and Fig. 9.

Fault detection logic for CHBMLI shown in Fig. 10 is based on average values (*mVOA, mVOB, mVOC*) of individual modules [4]. The fault detection logic decides the mode of operation by producing signals (MA, MB, MC) as shown in TABLE IV. In Mode-0; output voltage waveforms is symmetrical having average value equals to zero. During faulty conditions; module output gives non-zero average voltage due to asymmetrical output voltage waveform across the faulty module. When any module is faulty; relay operational logic and sector-based PWM logic will be changed according to the mode of operation as per TABLE IV. Simulink model of relay operational logic and sector based PWM logic have not shown in this paper due to limitation of space.

A. *Mode-0 to Mode-1*

As shown in TABLE IV; when Module-A gets faulty; CHBMLI operates in Mode-1. In this mode; source of the faulty Module-A is connected in series with the source of the healthy Module-B. In this way; the source of Module-B is $2V_{dc}$ and the source of Module-C is V_{dc}. Switching of IGBTs of various modules under Mode-1 is shown in TABLE V to generate 7-level output voltage. This can be validated from Fig. 11. Mode-0 is observed up to 0.4s. Fault occurs in Module-A at 0.4s. Non-uniform power sharing has been observed among three modules due to LS-PWM strategy of switching. Module-A is bypassed by operating RS1. The source of Module-A is connected in series with the source of Module-B by operating RS2, RS3, RD1, RD3 and RD5. It takes only half cycle to tolerate the fault. Output voltage waveform and its amplitude remain same.

TABLE IV. FAULT DETECTIN LOGIC

MA	MB	MC	Operation
0	0	0	Mode-0
1	0	0	Mode-1
0	1	0	Mode-2
0	0	1	Mode-3

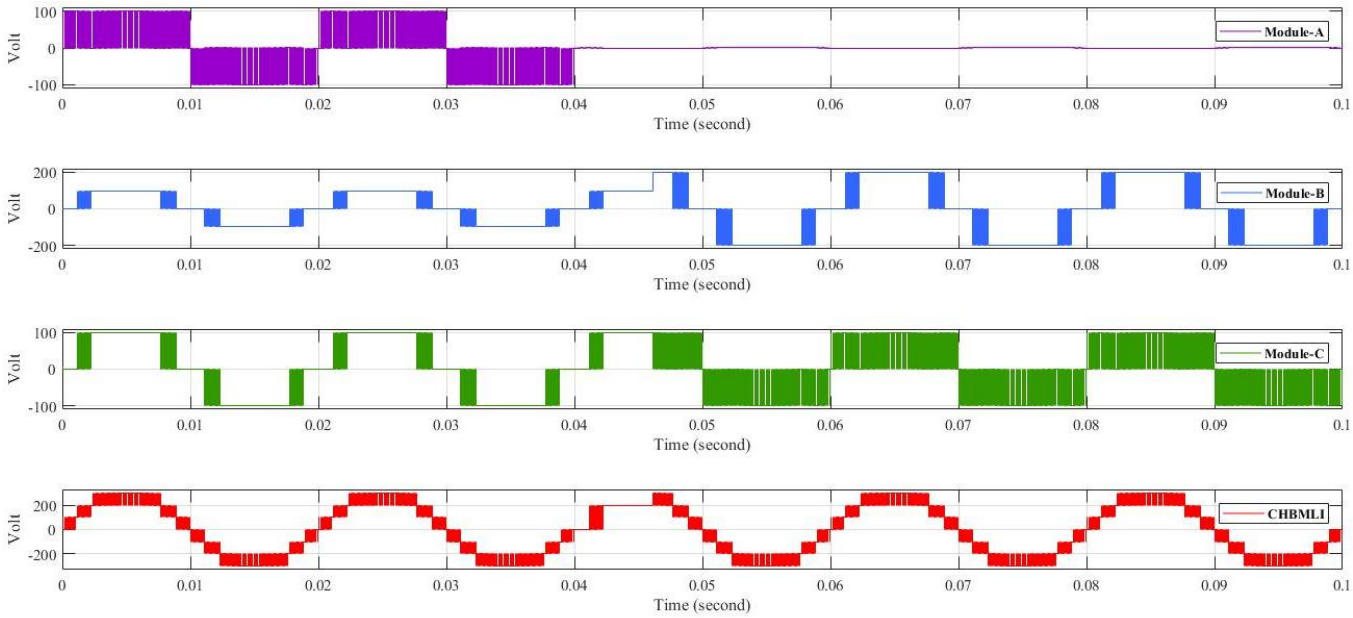


Fig. 11. (i) Module-A output voltage, (ii) Module-B output voltage, (iii) Module-C output voltage and (iv) CHBMLI output voltage under Mode-1

TABLE V. SWITCHING OF IGBTS UNDER MODE-1

Sector ↓	Module-A (Faulty)				Module-B (Healthy)				Module-C (Healthy)				Voltage Level
	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	
S1	0	0	0	0	1	1	0	0	1	1	0	0	+3Vdc
S2	0	0	0	0	1	1	0	0	0	1	0	1	+2Vdc
S3	0	0	0	0	0	1	0	1	1	1	0	0	+Vdc
S4	0	0	0	0	0	1	0	1	0	1	0	1	0
S5	0	0	0	0	0	1	0	1	0	1	0	1	0
S6	0	0	0	0	0	1	0	1	0	0	1	1	-Vdc
S7	0	0	0	0	0	0	1	1	1	0	1	0	-2Vdc
S8	0	0	0	0	0	0	1	1	0	0	1	1	-3Vdc

B. *Mode-0 to Mode-2*

When Module-B gets faulty; CHBMLI operates in Mode-2. Module-B is bypassed by operating RS4. The source of Module-B is connected in series with the source of Module-C by operating RS3, RS5, RD4, RD6 and RD8. In this way; the source of Module-C is $2V_{dc}$ and the source of Module-A is V_{dc}. Switching of IGBTs of various modules under Mode-2 is shown in TABLE VI to generate 7-level output voltage. Fig. 12 shows transition from Mode-0 to

Mode-2. Fig. 12 shows occurrence of fault in Module-B at 0.4s. Asymmetrical configuration of two healthy modules has possibility to generate 7-levels output voltage which is shown in Fig. 12. Transition period has been observed for a very short duration of less than a half cycle and hence acceptable.

C. Mode-0 to Mode-3

When Module-C gets faulty; CHBMLI operates in Mode-3. Module-C is bypassed by operating RS6. The source of Module-C is connected in series with the source of Module-A by operating RS7, RD1, RD7, RD8 and RD9. In this way; the source of Module-A is $2V_{dc}$ and the source of Module-B is V_{dc}. Switching of IGBTs of various modules under Mode-3 is shown in TABLE VII to generate 7-level output voltage. It shows that proposed fault-tolerant structure for CHBMLI can be used for continuous operation even during fault conditions.

In this project, the fundamental and most important consideration is the impact on continuity and reliability of inverter. During faulty condition; as the source of faulty module is utilized to maintain the output voltage waveform and its amplitude; IGBTs should be selected to handle twice the voltage stress experienced in normal operation.

III. Conclusion

Preserving the health of an inverter provides a basis for achieving higher reliability, survivability and productivity in industrial processes and energy systems. Proposed fault-tolerant structure for CHBMLI is able to continue operation with same output voltage waveform and amplitude; even if any 1 module becomes faulty. During normal operation; none of the relays in CHBMLI needs to be operated; while during faulty condition 6 relays are operated for isolation of faulty module and continue operation with same voltage magnitude. Fault detection logic developed in this paper are able to mitigate transition effect which has been observed while connecting source of faulty module with one of the healthy modules. Transition period from healthy operation to faulty operation of CHBMLI observed to be very short duration of less than a half cycle.

References

[1] Wenping Zhang, Dehong Xu, Prasad N. Enjeti, Haijin Li, Joshua T. Hawke, and Harish S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[2] Samir Kouro, Mariusz Malinowski, K. Gopakumar, Josep Pou, Leopoldo G. Franquelo, BinWu, Jose Rodriguez, Marcelo A. Pérez, and Jose I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] Marcelo A. Perez, Steffen Bernet, Jose Rodriguez, Samir Kouro, and Ricardo Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4-17, Jan. 2015.

[4] Anjali Anand, Nithin Raj, Saly George, and Jagadanand G., "Open switch fault detection in cascaded H-bridge multilevel inverter using normalised mean voltages," in *Proc. IEEE 6th International Conference on Power Systems (ICPS 2016)*, Apr. 2016, pp. 764–775.

[5] Pablo Lezana, Josep Pou, Thierry A. Meynard, Jose Rodriguez, Salvador Ceballos, and Frédéric Richardeau, and Luis Romeral, "Survey on Fault Operation on Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2207-2218, Jul. 2010.

[6] Haitham Abu-Rub, Joachim Holtz, Jose Rodriguez, and Ge Baoming, "Medium-voltage multilevel converters - state of the art, challenges, and requirements in industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[7] Behrooz Mirafzal, "Survey of Fault-Tolerance Techniques for Three-Phase Voltage Source Inverters," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5192–5202, Oct. 2014.

[8] Mohammad Mehdi Haji-Esmaeili, Mersad Naseri, Hossein Khoun-Jahan, and Mehdi Abapour, "Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation," *IET Power Electronics*, vol. 10, iss. 1, pp. 59-70, Jan. 2017.

[9] Hossein Khoun Jahan, Farhad Panahandeh, Mehdi Abapour, and Sajjad Tohidi, "Reconfigurable multilevel inverter with fault-tolerant ability," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7880-7893, Sep. 2018.

[10] Seok-Min Kim, June-Seok Lee, and Kyo-Beum Lee, "A modified level-shifted PWM strategy for fault-tolerant cascaded multilevel inverters with improved power distribution," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7264-7274, Nov. 2016.

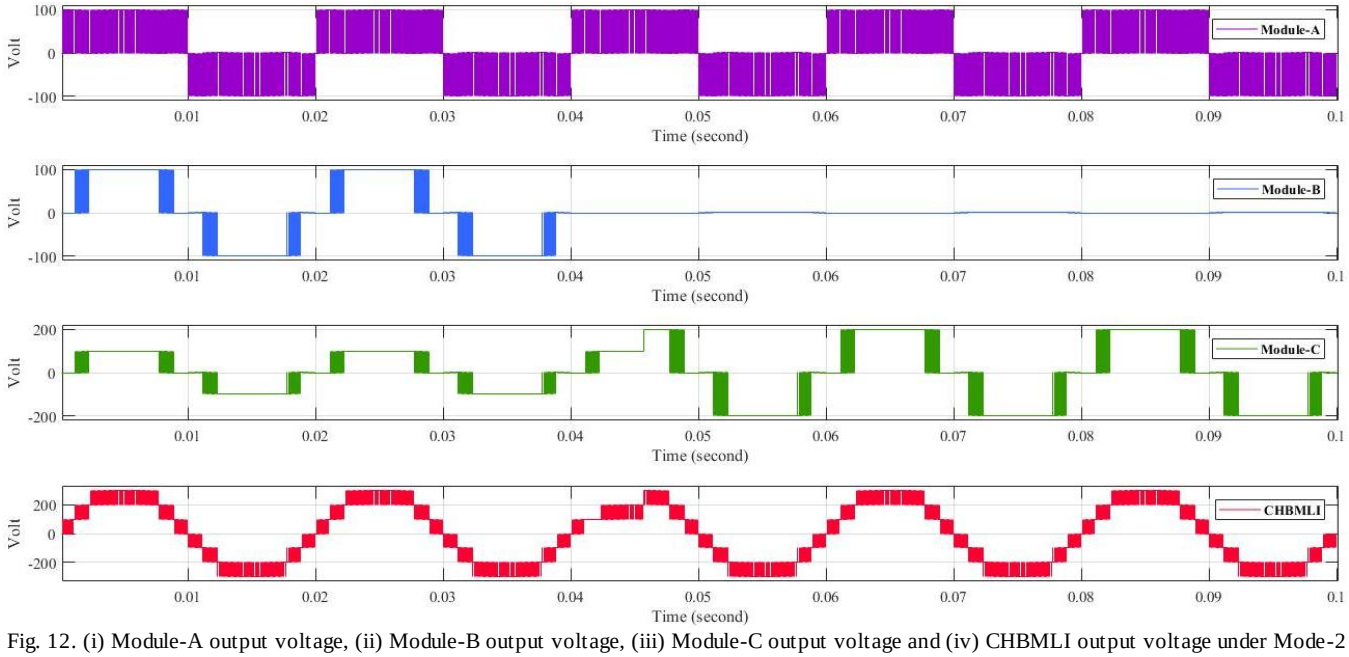


Fig. 12. (i) Module-A output voltage, (ii) Module-B output voltage, (iii) Module-C output voltage and (iv) CHBMLI output voltage under Mode-2

TABLE VI. SWITCHING OF IGBTS UNDER MODE-2

State ↓	**Module-A** (Healthy)				**Module-B** (Faulty)				**Module-C** (Healthy)				**Voltage Level**
	A1	**A2**	**A3**	**A4**	**B1**	**B2**	**B3**	**B4**	**C1**	**C2**	**C3**	**C4**	
S1	1	1	0	0	0	0	0	0	1	1	0	0	+3Vdc
S2	1	0	1	0	0	0	0	0	1	1	0	0	+2Vdc
S3	1	1	0	0	0	0	0	0	1	0	1	0	+Vdc
S4	0	1	0	1	0	0	0	0	1	0	1	0	0
S5	0	1	0	1	0	0	0	0	1	0	1	0	0
S6	0	0	1	1	0	0	0	0	1	0	1	0	-Vdc
S7	1	0	1	0	0	0	0	0	0	0	1	1	-2Vdc
S8	0	0	1	1	0	0	0	0	0	0	1	1	-3Vdc

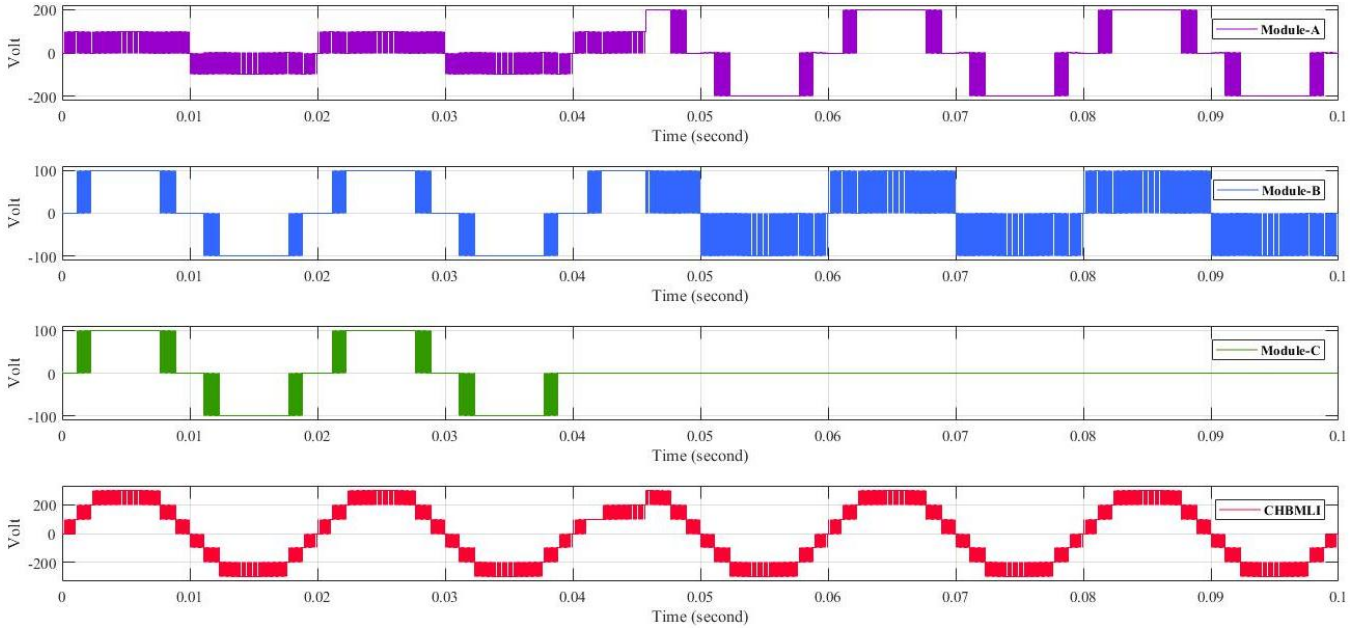
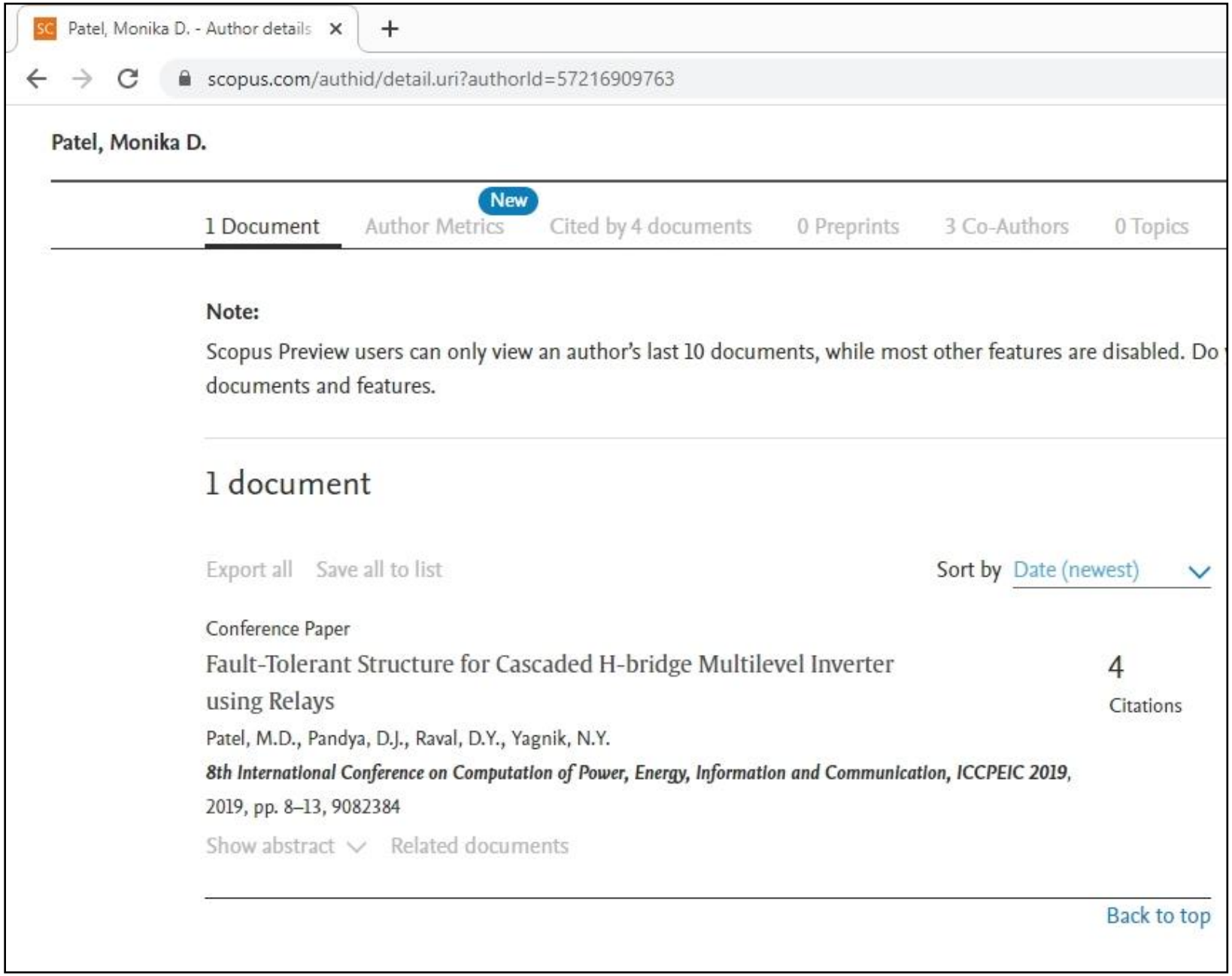


Fig. 13. (i) Module-A output voltage, (ii) Module-B output voltage, (iii) Module-C output voltage and (iv) CHBMLI output voltage under Mode-3

TABLE VII. SWITCHING OF IGBTS UNDER MODE-3

State ↓	**Module-A** (Healthy)				**Module-B** (Healthy)				**Module-C** (Faulty)				**Voltage Level**
	A1	**A2**	**A3**	**A4**	**B1**	**B2**	**B3**	**B4**	**C1**	**C2**	**C3**	**C4**	
S1	1	1	0	0	1	1	0	0	0	0	0	0	+3Vdc
S2	1	1	0	0	1	0	1	0	0	0	0	0	+2Vdc
S3	1	0	1	0	1	1	0	0	0	0	0	0	+Vdc
S4	0	1	0	1	0	1	0	1	0	0	0	0	0
S5	0	1	0	1	0	1	0	1	0	0	0	0	0
S6	0	1	0	1	0	0	1	1	0	0	0	0	-Vdc
S7	0	0	1	1	0	1	0	1	0	0	0	0	-2Vdc
S8	0	0	1	1	0	0	1	1	0	0	0	0	-3Vdc


Patel, Monika D. - Author details
scopus.com/authid/detail.uri?authorId=57216909763
Patel, Monika D.
1 Document
New
Author Metrics
Cited by 4 documents
0 Preprints
3 Co-Authors
0 Topics
Note:
Scopus Preview users can only view an author's last 10 documents, while most other features are disabled. Do
documents and features.
1 document
Export all
Save all to list
Sort by
Date (newest)
Conference Paper
Fault-Tolerant Structure for Cascaded H-bridge Multilevel Inverter using Relays
4
Citations
Patel, M.D., Pandya, D.J., Raval, D.Y., Yagnik, N.Y.
8th International Conference on Computation of Power, Energy, Information and Communication, ICCPEIC 2019,
2019, pp. 8–13, 9082384
Show abstract
Related documents
Back to top

Fault-Tolerant Structure for Cascaded H-bridge Multilevel Inverter for Double Module Faults

Monika D. Patel[*1], D. J. Pandya[2], Dhaval Y. Raval[3] and Niral Yagnesh Yagnik[4]

[1]Research Scholar, Department of Electrical Engineering, Atmiya University, Rajkot, India

[2]Associate Professor, Department of Electrical Engineering, Atmiya University, Rajkot, India

[3]Assistant Professor, Department of Electrical Engineering, Atmiya University, Rajkot, India

[4]Assistant Professor, Department of Electrical Engineering, Ganpat University, Mehsana, India

Abstract: *A fault-tolerant structure is proposed for Cascaded H-Bidge Multi-Level Inverters (CHBMLI) consisting of three modules. In the event that one module becomes faulty, the remaining two healthy modules will continue to deliver output voltage with the same amplitude and voltage level as during normal operation when all three modules are healthy. If two modules develop faults, the remaining single healthy module will still provide output voltage with the same amplitude, although at a reduced voltage level. This proposed fault-tolerant structure for CHBMLI enhances system reliability by preventing a complete breakdown of the entire system, ensuring that it continues to operate as long as at least one module remains in working condition. In this paper, the circuit operation under the double module faults is addressed.*

Keywords: **fault detection, fault tolerant, cascaded H-bridge, multilevel inverter, LS-PWM**

1. Introduction

Multi-level inverters, due to their utilization of a significant number of power switching devices, are more susceptible to switch faults. It is imperative to implement a swift and precise fault detection system to enhance the reliability of drives powered by multi-level inverters. Common switching device faults include short-switch faults and open-switch faults. In the event of a fault, traditional protection measures such as fuses, circuit breakers, and relays result in a complete shutdown of the drive system, which is not a desirable solution. Therefore, a systematic fault diagnostic scheme becomes essential for achieving fault-tolerant operation and designing an optimal protection strategy. Multilevel cascaded H-bridge inverter consists of series connected H-bridges. A cascadedinverter with N number of similar DC sources gives $(2N+1)$ levels at the output phase voltage. Figure 1 shows a single phase 7-level cascaded multilevel inverter. In the symmetric inverter in Fig.1.1 uses three separate voltage sources having equal magnitude $V_A = V_B = V_C = V_{dc}$.

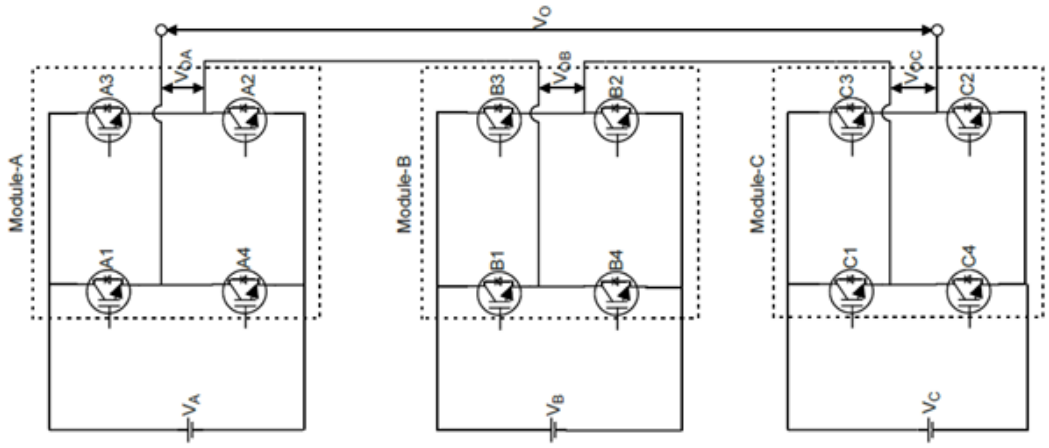


Figure 1. Classical cascaded H-bridge multilevel inverter

2. Proposed Fault Tolerant Structure for CHBMLI

Cascaded H-bridge multilevel inverter is basically a series connected multiple H-bridges [10]-[11]. If N number of modules with similar DC source gets connected in series, the overall configuration provides (2N+1) levels in output phase voltage [12]. Conventional single phase 7-level CHBMLI is shown in Figure 1.It has 3 modules *viz.* Module-A, Module-B and Module-C. To generate 7-level output voltage; CHBMLI uses 3 separate voltage sources having equal magnitude*i.e.*$V_A = V_B = V_C = V_{dc}$[13]. In Figure 1, A1-A4, B1-B4 and C1-C4 are IGBTs forming 3 H-bridges. V_{OA}, V_{OB} and $V_{OC}$are instantaneous output voltages of individual modules. V_O represents total instantaneous output voltage of CHBMLI.

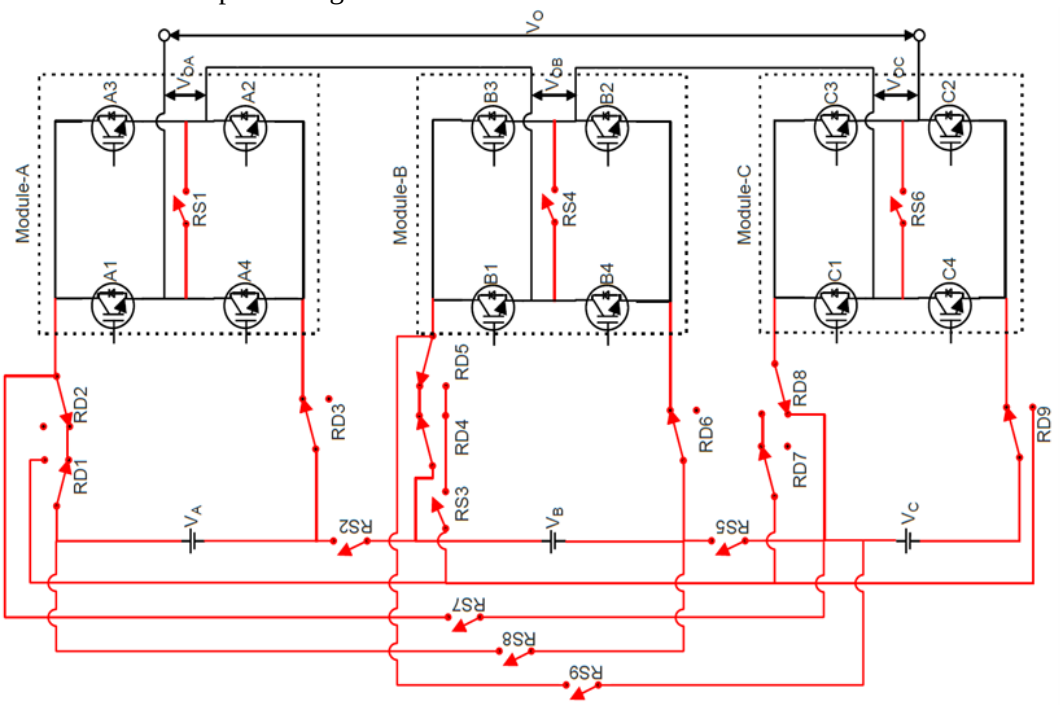


Figure 2. Proposed fault-tolerant structure for CHBMLI

The proposed fault-tolerant structure for a seven-level CHBMLI is depicted in Figure 2. Additional 16 relays are utilised to reroute current flow in the case of a failure in any semi-conductor switch. RS1-RS7 in Fig. 2 are single pole single throw (SPST) relays, whereas RD1-RD9 are single pole double throw (SPDT) relays. When a single module becomes faulty, CHBMLI continues to operate by taking two steps: (i) isolating the faulty module and (ii) connecting the source of the faulty module to one of the sources of healthy modules. Table I displays the various modes of operation for the proposed fault-tolerant CHBMLI. In Table 1, H represents a module in a healthy condition and F represents a module in a faulty condition. Mode-0 is the usual state of CHBMLI. Mode-1, Mode-2, and Mode-3 are faulty states of CHBMLI.

Table 1. Operating Modes

Module A	Module B	Module C	Operation	
H	H	H	Mode-0	All Modules Healthy
F	H	H	Mode-1	One Module Faulty
H	**F**	H	Mode-2	
H	H	**F**	Mode-3	
F	**F**	H	Mode-4	Two Modules Faulty
H	**F**	**F**	Mode-5	
F	H	**F**	Mode-6	

Table 2 demonstrates relay state for each mode of operation. 0 represents an inactive or unchanging state, while 1 indicates an active or modified state. In Mode-0, all relays are in their resting state. When a single module becomes faulty, six of sixteen relays are activated to isolate the faulty module and utilise its source. CHBMLI, which normally operates in a symmetrical configuration, switches to an asymmetrical configuration in the event of a fault in order to provide a 7-level output voltage with the same voltage amplitude. RS1 to RS9 are SPST relays. RD1 to RD9 are SPDT relays. '1' indicates that a particular relay is operated and '0' indicates a particular relay is not operated.

Table 2. Operating Modes

RELAY	MODE-0 A=H, B=H, C=H	MODE-1 A=F, B=H, C=H	MODE-2 A=H, B=F, C=H	MODE-3 A=H, B=H, C=F	MODE-4 A=F, B=F, C=H	MODE-5 A=H, B=F, C=F	MODE-6 A=F, B=H, C=F
RS1	0	1	0	0	1	0	1
RS2	0	1	0	0	1	0	1
RS3	0	1	1	0	0	1	0
RS4	0	0	1	0	1	1	0
RS5	0	0	1	0	1	0	0
RS6	0	0	0	1	0	1	1
RS7	0	0	0	1	0	1	0
RS8	0	0	0	0	0	1	0
RS9	0	0	0	0	0	0	1
RD1	0	1	0	1	1	0	1
RD2	0	0	0	0	0	1	0
RD3	0	1	0	0	1	0	1
RD4	0	0	1	0	0	1	0
RD5	0	1	0	0	1	0	1
RD6	0	0	1	0	1	1	0
RD7	0	0	0	1	0	1	1
RD8	0	0	1	1	1	1	1
RD9	0	0	0	1	0	1	1
TOTAL	0	6	6	6	9	11	10

3. Operation under Double Module Faults

When Module-A & Module-B are faulty, Module-C remains in operating condition. Modified structure of CHBMLI in Mode-4 is shown in Figure 3. RS1, RD3 and RS4, RD5, RD6 are operated to isolate Module-A and Module-B respectively. To maintain the output voltage magnitude same as in healthy condition sources of Module-A and Module-B utilized along with the source of Module-C. RD1 are operated to connect source of Module-A to Module-C.RS2 and RS5 are operated to connect voltage sources of Module-C and Module-B in series with Module-A. Series connection of all three sources provide $3V_{dc}$ input voltage to Module-C. All the operated relays are highlighted in Figure 3.

When Module-B & Module-C become faulty, Module-A remains in operating condition. Modified structure of CHBMLI in Mode-5 is shown in Figure 4. RS4, RD6 and RS6, RD7, RD8 are operated to isolate Module-B and Module-C respectively. To maintain the output voltage magnitude same as in healthy condition sources of Module-B and Module-C utilized along with the source of Module-A. RS3, RD4 and RD9 are operated to connect source of Module-B to Module-C. RS8 are operated to connect voltage sources of Module-A in series with Module-B. RS7 is operated to connect source of Module-C with Module-A. Series connection of all three sources provide $3V_{dc}$ input voltage to Module-A. All the operated relays are highlighted in Figure 4.

When Module-A & Module-C become faulty, Module-B remains in operating condition. Modified structure of CHBMLI in Mode-6 is shown in Figure 5. RS1, RD3 and RS6, RD7, RD8 are operated to isolate Module-A and Module-C respectively. To maintain the output voltage magnitude same as in healthy condition sources of Module-A and Module-C utilized along with the source of Module-B. RD5 is utilized to isolate source of Module-B and RS2 is operated to connect it with source of Module-A. RD1 and RD9 are operated to connect source of Module-A with source of Module-C. Finally, RS9 connect

source of Module-C to Module-B. Series connection of all three sources provide $3V_{dc}$ input voltage to Module-B. All the operated relays are highlighted in Figure 5.

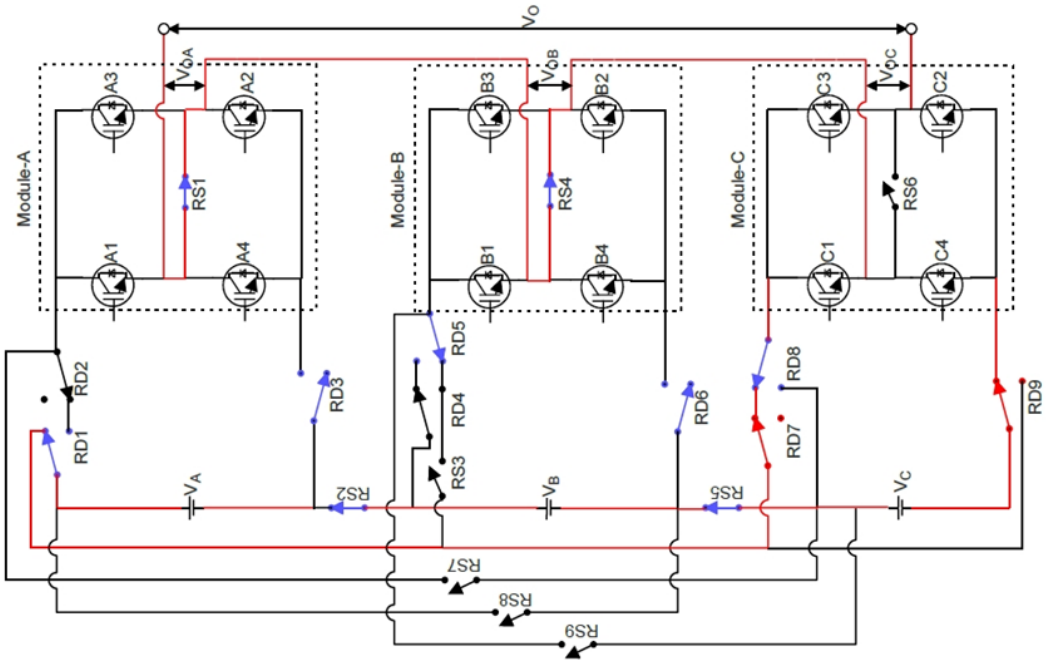


Figure 3. Current flow under Mode-4

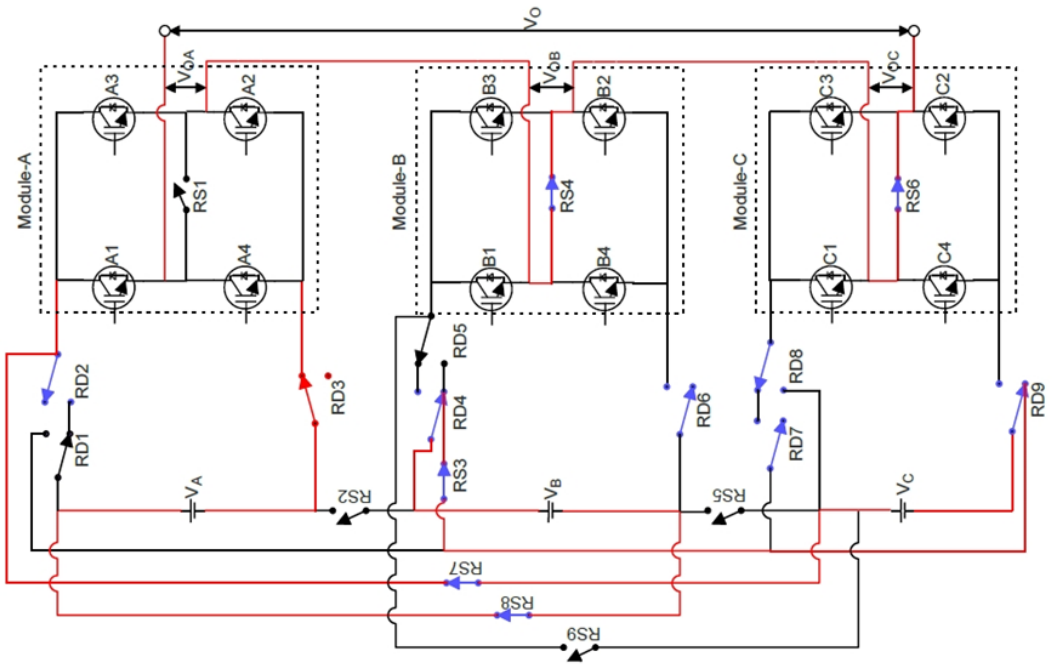


Figure 4. Current flow under Mode-5

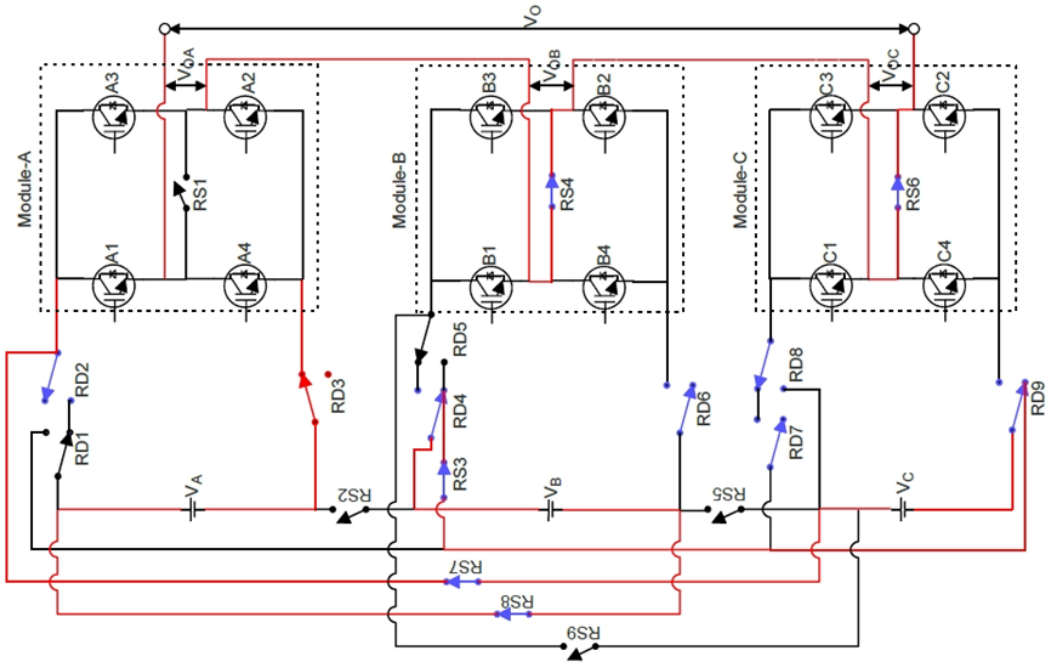


Figure 5. Current flow under Mode-6

4. Conclusion

The proposed fault-tolerant structure for CHBMLI can continue operating even when two modules are faulty. The operation of all the double module faults is represented by means of circuit diagram, current flow and operation of various relays. The proposed structure is to be simulated for further verification.

References

[1] Wenping Zhang, Dehong Xu, Prasad N. Enjeti, Haijin Li, Joshua T. Hawke, and Harish S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[2] Samir Kouro, Mariusz Malinowski, K. Gopakumar, JosepPou, Leopoldo G. Franquelo, BinWu, Jose Rodriguez, Marcelo A. Pérez, and Jose I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] Marcelo A. Perez, Steffen Bernet, Jose Rodriguez, Samir Kouro, and Ricardo Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4-17, Jan. 2015.

[4] Anjali Anand, Nithin Raj, Saly George, and Jagadanand G., "Open switch fault detection in cascaded H-bridge multilevel inverter using normalised mean voltages," in *Proc.IEEE 6th International Conference on Power Systems (ICPS 2016)*, Apr. 2016, pp. 764–775.

[5] Pablo Lezana, JosepPou, Thierry A. Meynard, Jose Rodriguez, Salvador Ceballos, and FrédéricRichardeau, and Luis Romeral, "Survey on Fault Operation on Multilevel Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2207-2218, Jul. 2010.

[6] Haitham Abu-Rub, Joachim Holtz, Jose Rodriguez, and Ge Baoming, "Medium-voltage multilevel converters - state of the art, challenges, and requirements in industrial applications," *IEEETransactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[7] BehroozMirafzal, “Survey of Fault-Tolerance Techniques for Three-Phase Voltage Source Inverters,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5192–5202, Oct. 2014.
[8] Mohammad Mehdi Haji-Esmaeili, MersadNaseri, Hossein Khoun-Jahan, and Mehdi Abapour, “Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation,” *IET Power Electronics*, vol. 10, iss. 1, pp. 59-70, Jan. 2017.
[9] Hossein Khoun Jahan, FarhadPanahandeh, Mehdi Abapour, and SajjadTohidi, “Reconfigurable multilevel inverter with fault-tolerant ability,” *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7880-7893, Sep. 2018.
[10] AV, Badgujar, et al. "A Comparative Analysis of Cascaded H-Bridge Multilevel Inverters and Envisaged Topologies." Available at SSRN 3884724 (2021).
[11] Faizan, Mohd, et al. "Performance Analysis of Five-Level-Cascaded H-Bridge Inverter." Renewable Power for Sustainable Growth. Springer, Singapore, 2021. 377-385.
[12] Balal, Afshin, et al. "A Review on Multilevel Inverter Topologies." Emerging Science Journal 6.1 (2022): 185-200.
[13] Thiyagarajan, V. "A novel 7-Level symmetric inverter module with less circuit components." Materials Today: Proceedings (2022).
[14] Seok-Min Kim, June-Seok Lee, and Kyo-Beum Lee, “A modified level-shifted PWM strategy for fault-tolerant cascaded multilevel inverters with improved power distribution,” *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7264-7274, Nov. 2016.

Source details

GIS-Zeitschrift fur Geoinformatik

Scopus coverage years: from 2006 to 2009, from 2011 to 2022

Publisher: Wichmann, VDE

ISSN: 1869-9391 E-ISSN: 2698-4571

Subject area: Social Sciences: Geography, Planning and Development | Computer Science: Information Systems

Source type: Journal

View all documents > | Set document alert | Save to source list | Source Homepage

CiteScore 2015
0.1

SJR 2017
0.100

SNIP 2017
0.000

CiteScore | CiteScore rank & trend | Scopus content coverage

¡ Improved CiteScore methodology

CiteScore 2015 counts the citations received in 2012-2015 to articles, reviews, conference papers, book chapters and data papers published in 2012-2015, and divides this by the number of publications published in 2012-2015. Learn more >

CiteScore 2015

$$0.1 = \frac{6 \text{ Citations 2012 - 2015}}{78 \text{ Documents 2012 - 2015}}$$

Calculated on 01 May, 2016

CiteScoreTracker 2023

$$0.6 = \frac{23 \text{ Citations to date}}{40 \text{ Documents to date}}$$

Last updated on 05 December, 2023 • Updated monthly

CiteScore rank 2015

Category	Rank	Percentile
Social Sciences └ Geography, Planning and Development	#547/584	6th
Computer Science └ Information Systems	#230/233	1st

View CiteScore methodology > | CiteScore FAQ > | Add CiteScore to your site