# Chapter 1
# Introduction

## 1.1 Introduction

Multilevel inverters have become an essential component in high-power industrial drive systems. They offer numerous advantages over conventional two-level inverters, such as higher quality output voltage, lower distortion in input current, reduced switching frequency, diminished voltage stress on power switches, and smaller common-mode voltage, making them highly desirable. Additionally, multilevel inverters facilitate the integration of renewable energy sources into AC drive systems.

Among the various topologies of multilevel inverters, the most widely used options are Diode Clamped or Neutral-Point Clamped, Flying Capacitor or Capacitor Clamped, and Cascaded H-bridge. Of these, Cascaded H-Bridge Multi-Level Inverters (CHBMLI) are extensively employed in high-power medium voltage drives due to their modularity and increased power and voltage capabilities.

Cascaded inverters employ a series connection of single-phase H-Bridges with lower voltage DC sources to achieve higher power output. By appropriately controlling the power switches, the individual inverter outputs are synchronized to produce a high output voltage. However, the primary drawback of this topology is the requirement for multiple separate DC sources.

Multi-level inverters, due to their utilization of a significant number of power switching devices, are more susceptible to switch faults. It is imperative to implement a swift and precise fault detection system to enhance the reliability of drives powered by multi-level inverters. Common switching device faults include short-switch faults and open-switch faults. In the event of a fault, traditional protection measures such as fuses, circuit breakers, and relays result in a complete shutdown of the drive system, which is not a desirable solution. Therefore, a systematic fault diagnostic scheme becomes essential for achieving fault-tolerant operation and designing an optimal protection strategy.

Multilevel cascaded H-bridge inverter consists of series connected H-bridges. A cascaded inverter with $N$ number of similar DC sources gives $(2N+1)$ levels at the output phase voltage. Fig.1.1 shows a single phase 7-level cascaded multilevel inverter. In the symmetric inverter in Fig.1.1 uses three separate voltage sources having equal magnitude $V_A = V_B = V_C = V_{dc}$.

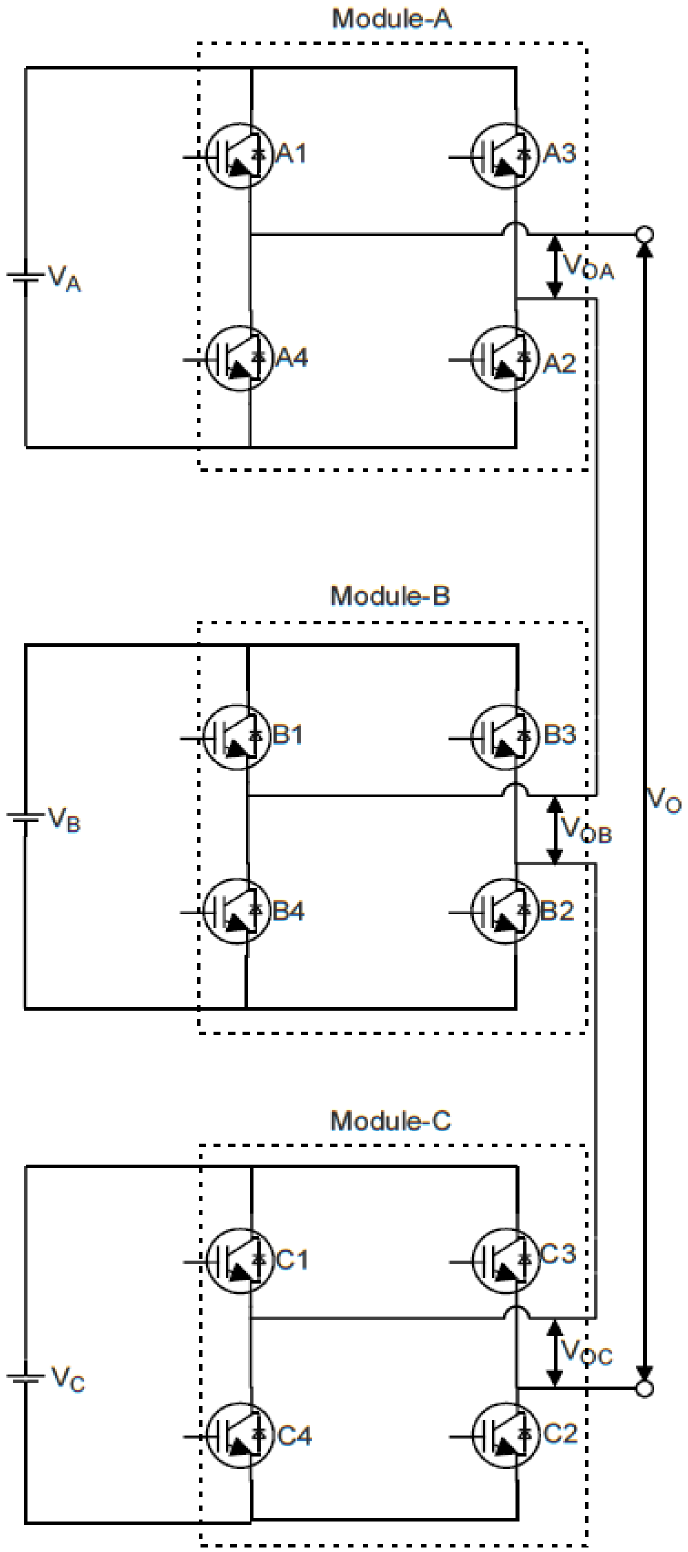


Figure1.1: Basic cascaded H-bridge multilevel inverter

## 1.2 Organization of the Thesis

The core research work is divided in 5 chapters of the thesis. Chapter-wise content covered is summarized as follows:

Chapter 2 encompasses literature review of various topics related to cascaded H-bridge multilevel inverter, followed by research gap.

In Chapter 3, a novel fault-tolerant structure for a cascaded H-bridge multilevel inverter is proposed to fulfill the research gaps found during the literature review. The proposed design is capable to keep the inverter in operation till any one module is healthy. The circuit operation is divided in 7 modes. Mode-0 is the normal operating condition of the inverter. Mode-1, Mode-2 and Mode-3 are single module faults. Mode-4, Mode-5 and Mode-6 are double module faults. In this chapter, all these modes are explained in detail.

Chapter 4 covers Simulation & Results. To validate the proposed fault-tolerant structure of cascaded H-bridge multilevel inverter, simulation study has been carried out using MATLAB/Simulink. In this chapter, various functional blocks, sub-systems and control logic are explained thoroughly. The proposed structure is verified by the results of simulation.

In Chapter 5, various components are discussed to develop the hardware of the proposed fault-tolerant structure of cascaded H-bridge multilevel inverter. The hardware is divided in major sections like Relay Card, Driver Card, IGBT Card and interfacing with Microcontroller. Hardware results are matching with the simulation results.

Reliability analysis is carried out in Chapter 6. Reliability is the probability that a circuit will perform its intended working for a specified period of time under normal operation. Markov evaluation approach is applied to calculate the reliability of the proposed hardware. It is found that the reliability of fault-tolerant cascaded H-bridge 7-level multilevel inverter is more as compare to the cascaded H-bridge 7-level multilevel inverter without any fault-tolerant arrangement.