Chapter 4

Simulation Results

To validate the proposed structure of FT-CHBMLI simulation study has been carried out using MATLAB/Simulink. Fig. 4.1 shows different subsystems to simulate FT-CHBMLI.

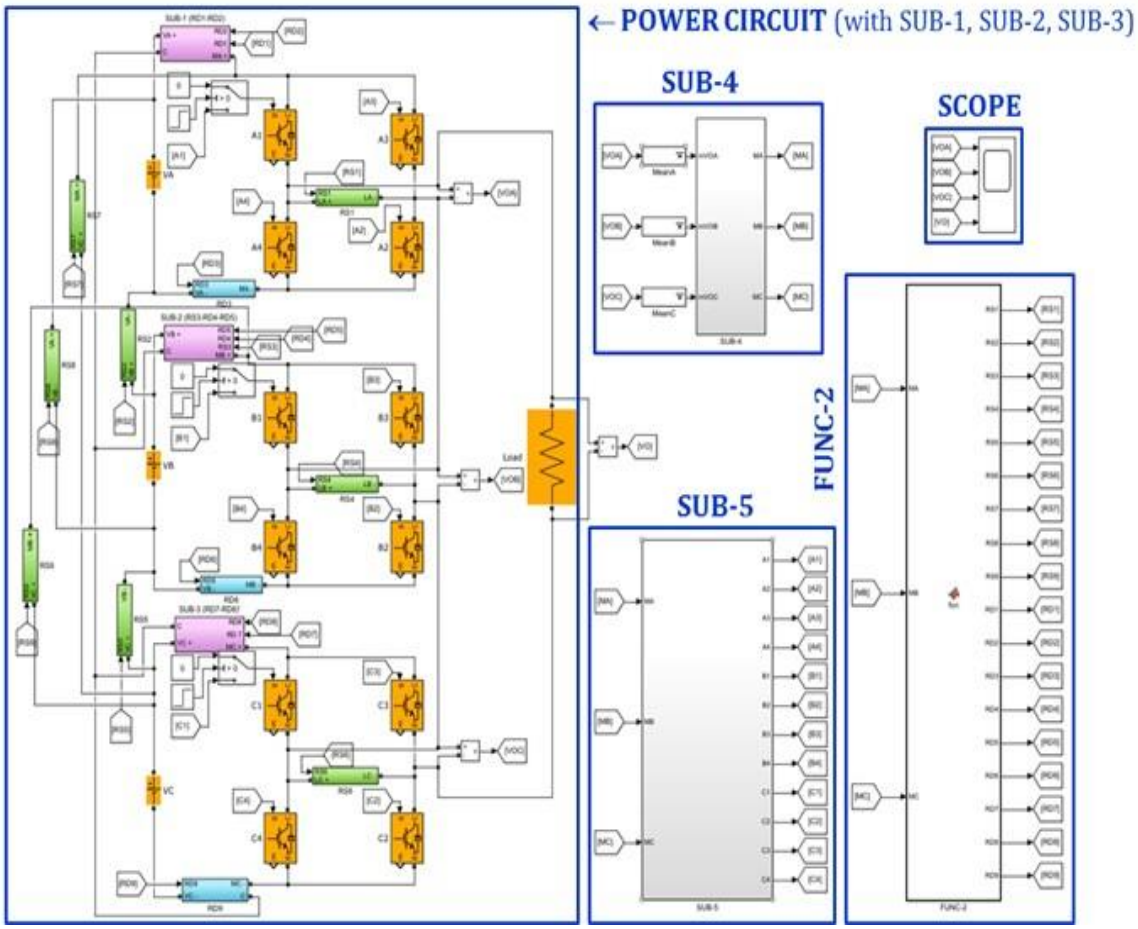


Figure 4.1: MATLAB Simulation

Fig. 4.1 include power circuit along with control circuit of FT-CHBMLI. SUB-1, SUB-2 and SUB-3 are the logical relays, combination of ordinary SPST/SPDT relays, which are the part of FT-CHBMLI power circuit. SUB-4, SUB-5 and FUNC-2 are the parts of control logic for FT-CHBMLI. SUB-4 is fault detection logic. SUB-5 is PWM generation logic and FUNC-2 is relay operation logic. Fault detection logic detect the fault and generate control signal M_A, M_B and M_C. PWM generation logic and Relay operation logic modify their output signals according to the status of M_A, M_B and M_C. Power Circuit and control logic are briefly explained in further section.

4.1 Power Circuit

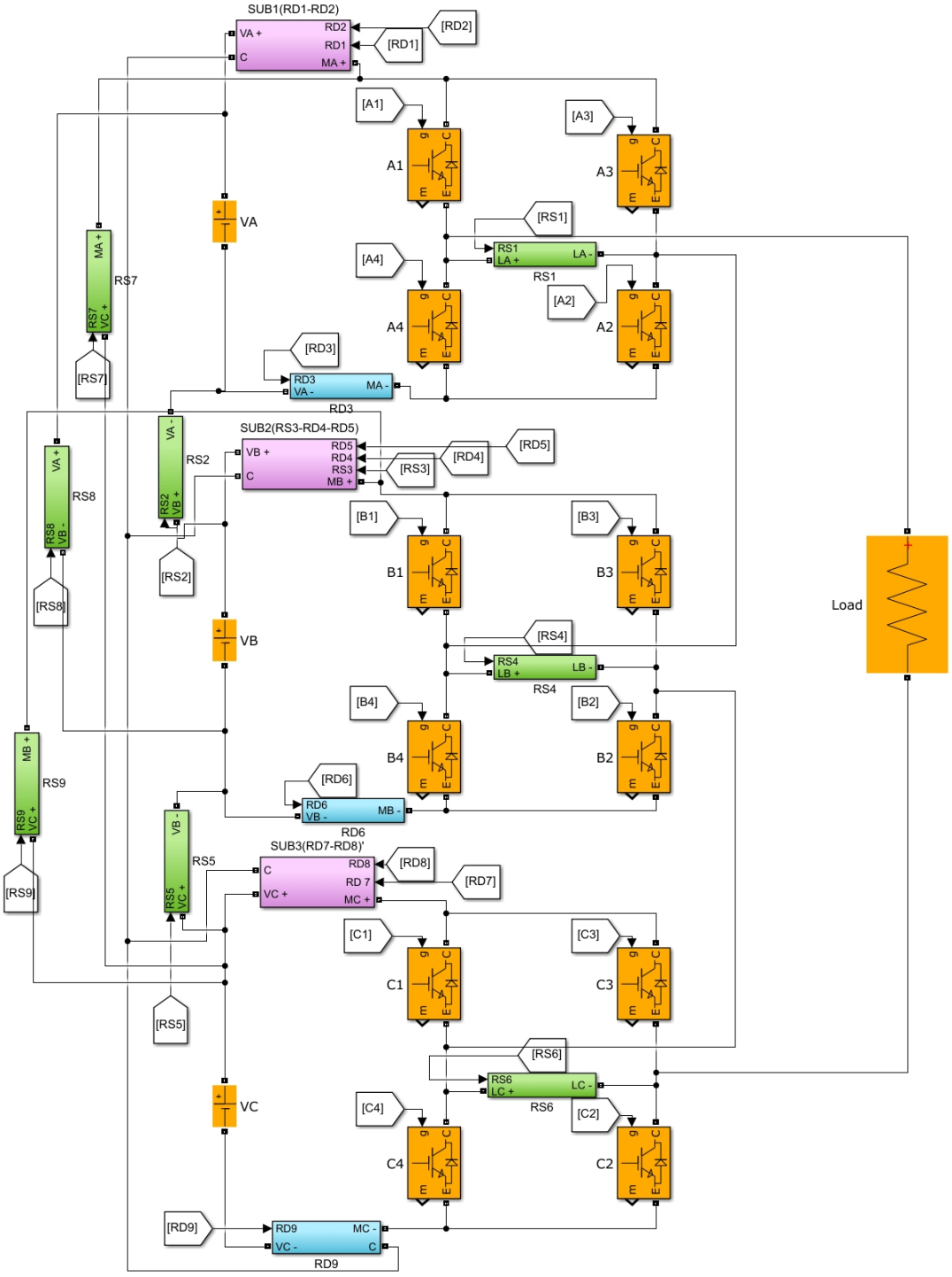
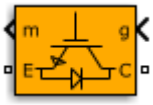


Figure 4.2: Power circuit with relays

Simulation diagram of Power Circuit is shown in Fig. 4.2. Three 100V DC sources are used to form symmetrical structure of 7 level CHBMLI. Color coding has been used to reduce the complexity of circuit. Table 4.1 shows different elements of power circuits. 12 IGBTs are utilized to form 7- Level CHBMLI. 9 SPST (Green) and 9 SPDT

(Light Blue) are used to realize fault tolerant structure of CHBMLI. SUB-1, SUB-2 and SUB-3 are combination of SPST and SPDT relays and known as logical relays. Fig. 4.3, Fig. 4.4 and Fig. 4.5 shows the connection diagram of these logical relays.

Table 4.1**:** List of elements

Element	Remarks
	**IGBT:** A1-A4, B1-B4, C1-C4
	**SPST Relay:** RS1-RS9
	**SPDT Relay:** RD1-RD9
	**Combinational Relay:** SUB-1, SUB-2, SUB-3
	**DC Voltage Sources:** VA, VB, VC

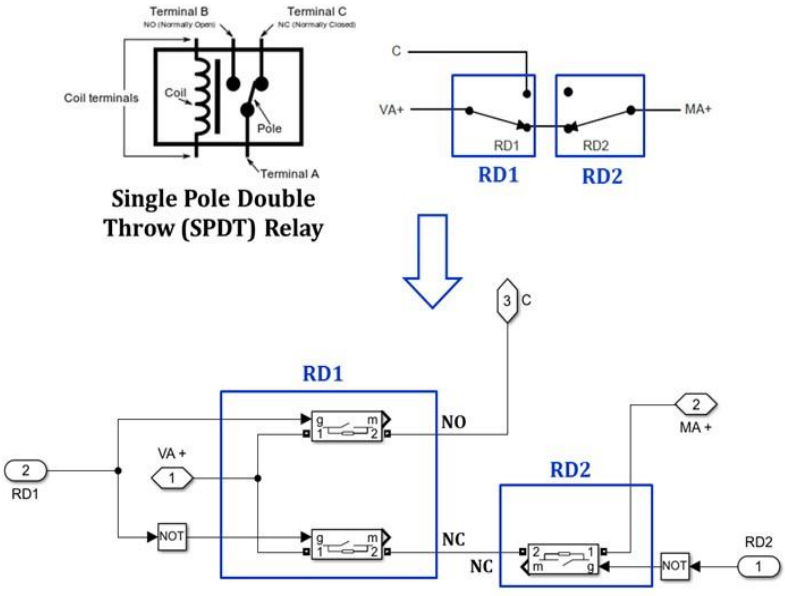


Figure 4.3: Sub system (SUB-1)

RD1	RD2	Connection
0	1	Isolated
0	0	(VA+) to (MA+)
1	0	(VA+) to (C)
1	1	

Table 4.2**:** Connection Possibility of Logical Relay in SUB-1

Connection possibility of logical relay in SUB-1 is shown in Table. 4.2. VA+, MA+, C notations are used to indicate positive terminal of source of Module-A, positive terminal of Module-A and common rail respectively. As per the mode of operation this logical relay changes its connection.

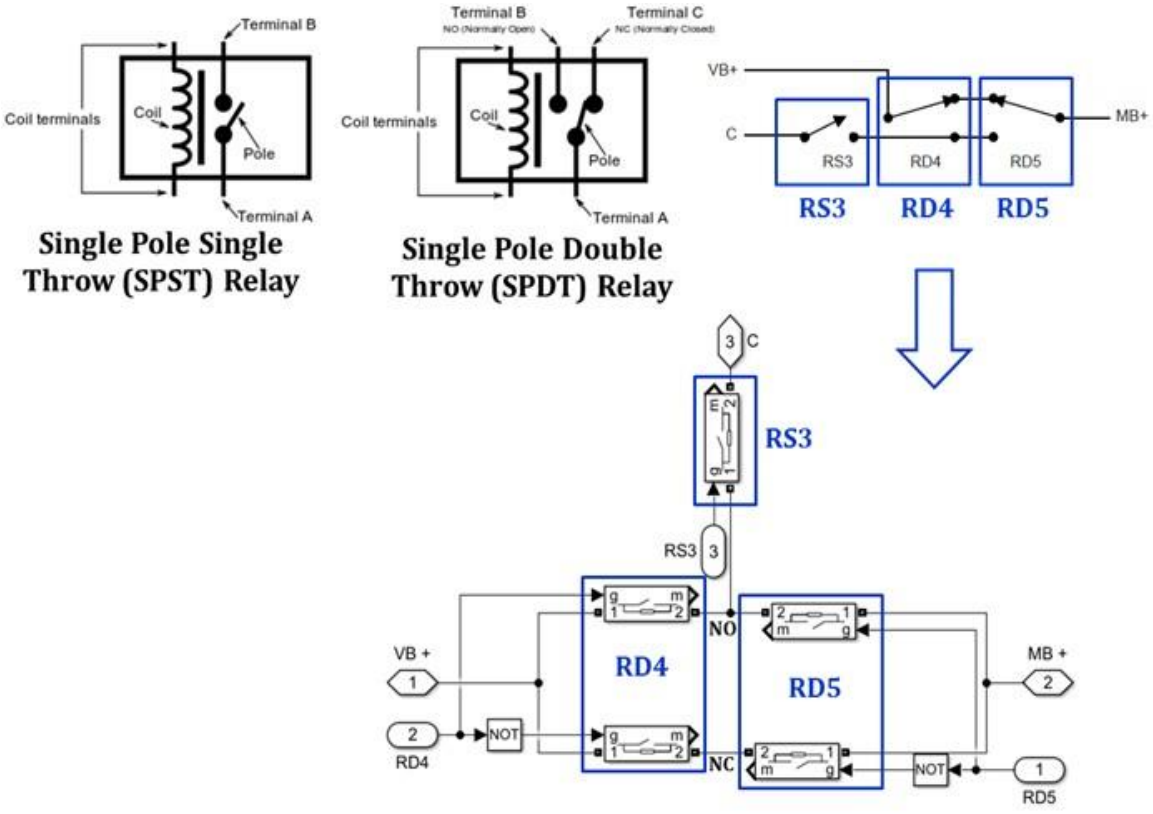


Figure 4.4: Sub system (SUB-2)

Connection possibility of logical relay in SUB-2 is shown in Table. 4.3. VB+ and MB+ notations are used to indicate +Ve terminal of source of Module-B and +Ve terminal of Module-B respectively. As per the mode of operation this logical relay changes its connection.

Connection possibility of logical relay in SUB-3 is shown in Table. 4.4. VC+ and MC+ notations are used to indicate +Ve terminal of source of Module-C and +Ve

terminal of Module-C respectively. As per the mode of operation this logical relay changes its connection.

RS3	RD4	RD5	Connection
0	0	1	Isolated
0	1	0	
0	0	0	(VB+) to (MB+)
0	1	1	
1	0	0	
1	0	1	(C) to (MB+)
1	1	0	
1	1	1	Not Allowed (SC)

Table 4.3 Connection Possibility of Logical Relay in SUB-2

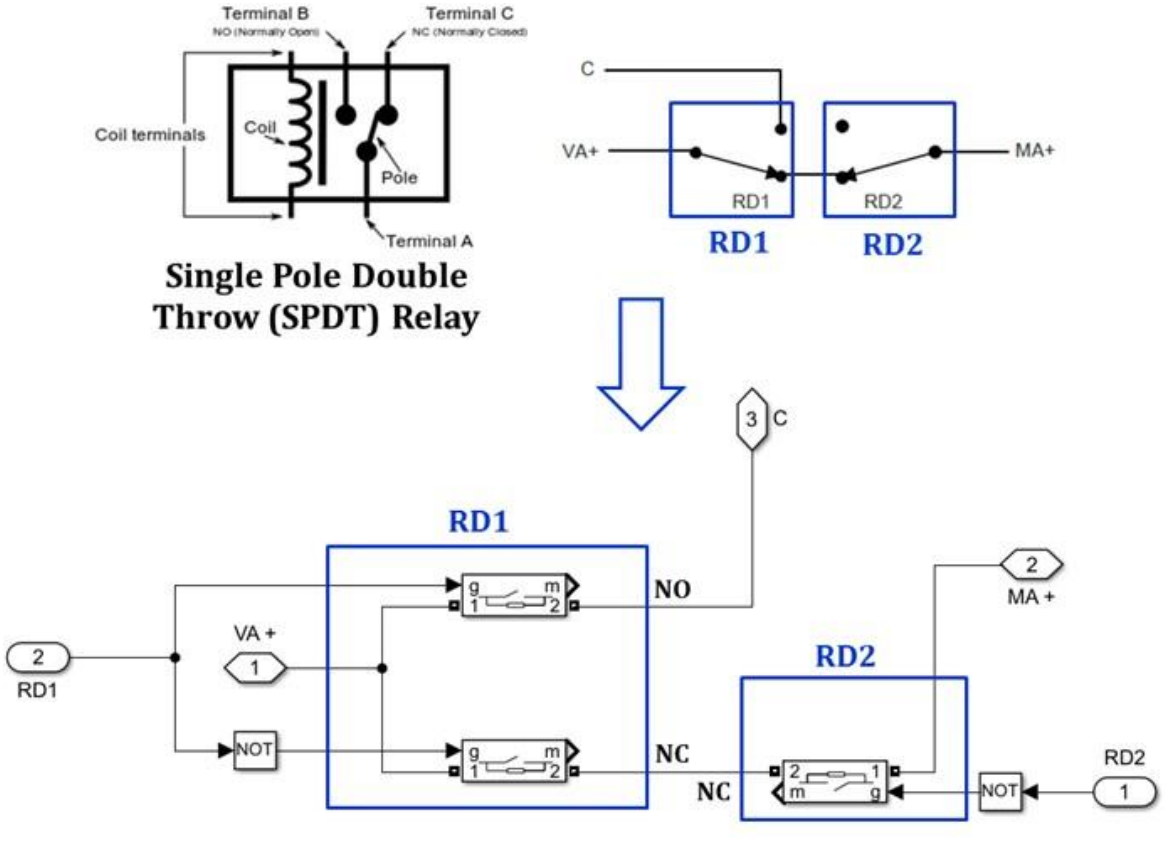


Figure 4.5: Sub system (SUB-3)

RD7	RD8	Connection
1	1	Isolated
0	0	(VC+) to (MC+)
1	0	
0	1	(C) to (MC+)

Table 4.4: Connection Possibility of Logical Relay in SUB-3

4.2 Fault Detection Logic (SUB-4)

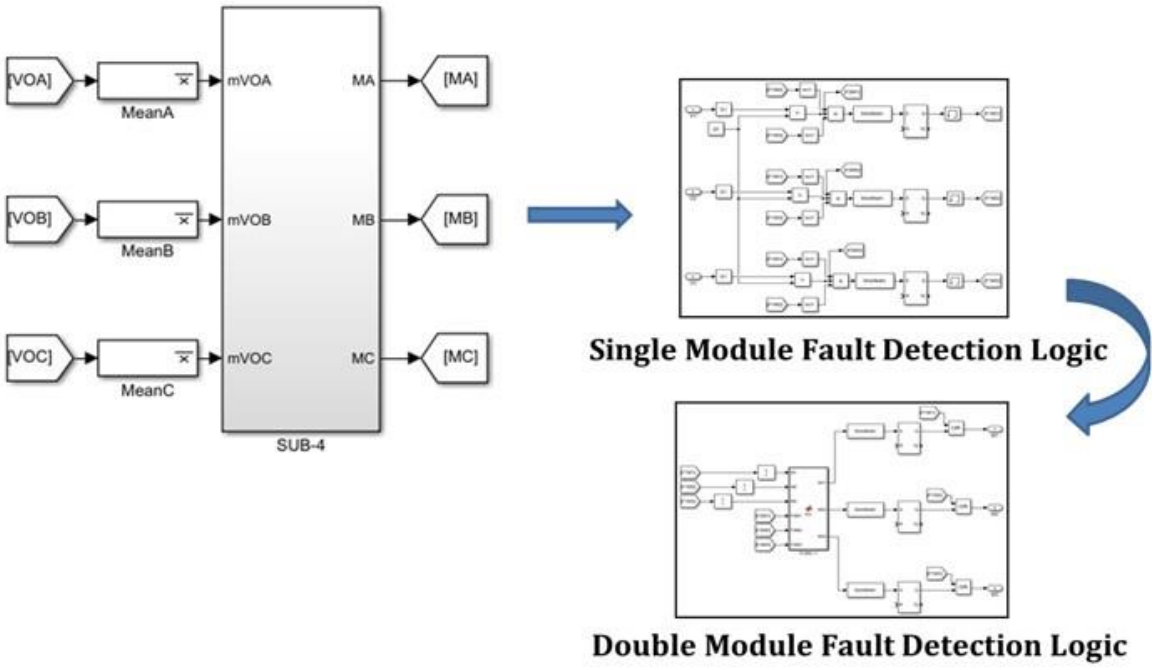


Figure 4.6: Sub system (SUB-4)

Fig.4.6 shows fault detection logic for FT-CHBMLI. Fault detection logic is divided in two parts:

1) Single Module Fault Detection
2) Double Module Fault Detection

Single module fault detection logic detects first fault in any one out of three modules. When any one module becomes faulty operation remains continue by remaining two healthy modules. If fault occur in any module out of this two, it will be termed as second module fault and get detected by double module fault detection logic. Double module fault detection logic depends on single module fault detection logic and get activated only after single module fault detect first fault.

Fig.4.7 shows single module fault detection logic. It works on average value of output voltage from individual module. In normal operation when all the modules are healthy, Individual bridge voltage are symmetrical in shape. Average value of these symmetrical voltage over one cycle becomes zero. When any switch of modules becomes faulty, it introduces asymmetry in output voltage. Average value of unsymmetrical voltage over one cycle being non-zero, get detected by single module

fault detection logic. Once any module considered to be faulty, single module fault detection logic does not response for any other fluctuation in output voltage of remaining healthy modules.

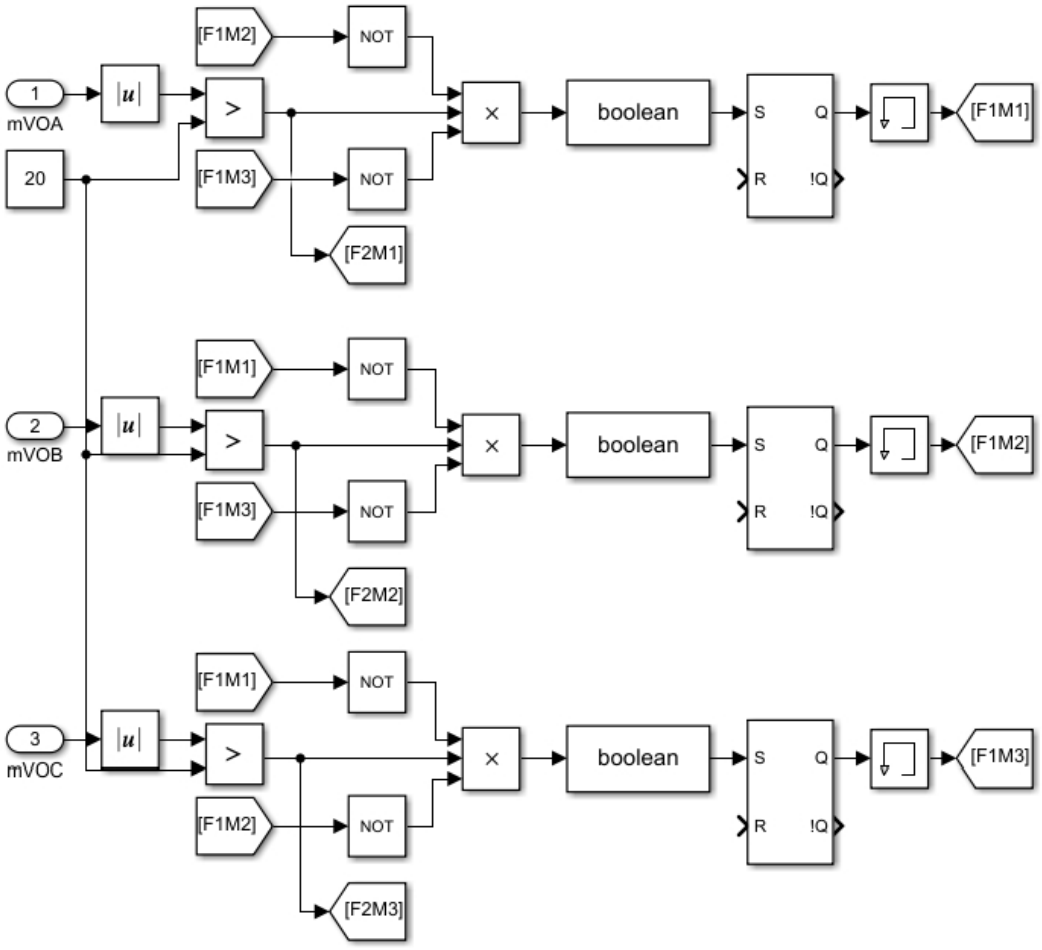


Figure 4.7: Single module fault detection logic

MA	MB	MC	Operation
0	0	0	Mode-0
1	0	0	Mode-1
0	**1**	0	Mode-2
0	0	**1**	Mode-3
1	**1**	0	Mode-4
0	**1**	**1**	Mode-5
1	0	**1**	Mode-6

0 = Healthy | **1** = Faulty Module

Table 4.5**:** Fault detection

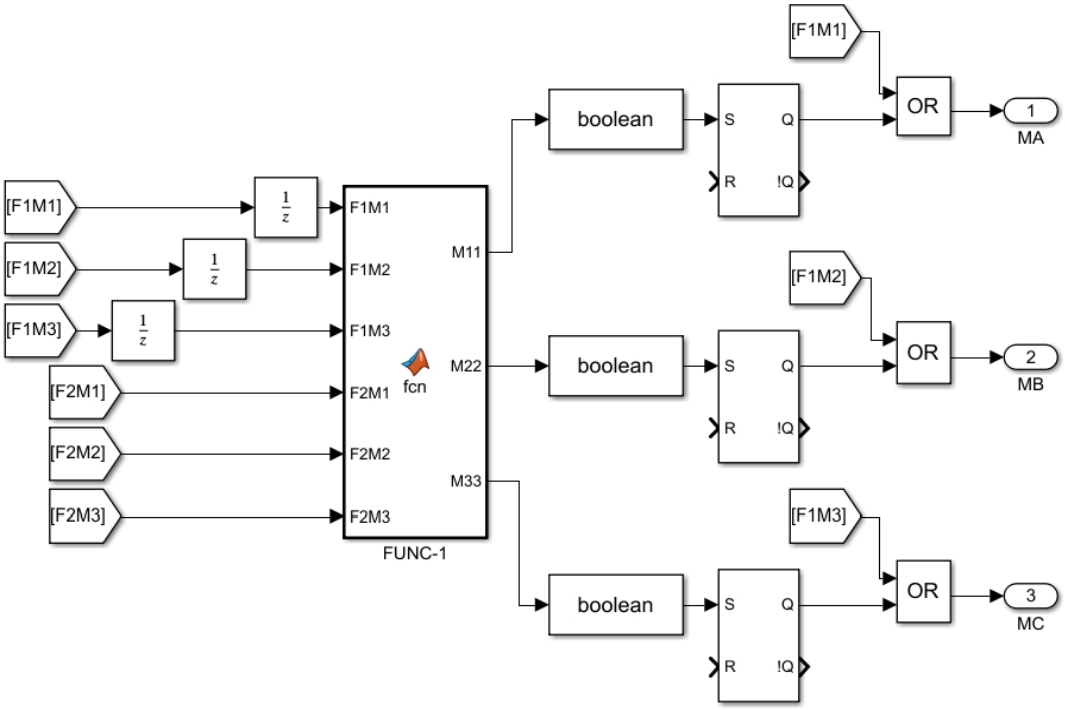


Figure 4.8: Double module fault detection logic

Double module fault detection logic is shown in Fig. 4.8. This logic gets activated if there is fault in any single module and FT-CHBMLI is operating with two healthy modules. Double module fault detection also works on the deviation of average value of individual modules. Finally, MA, MB and MC signals are generated by above described two fault detection logic which used to take action for fault tolerance. According do status of MA, MB and MC, different mode of operation is summarized in Table. 4.5.

4.3 Function block to operate respective relay

According to control signals MA, MB and MC relays should be operated according to Table. 4.2. Fig. 4.9 shows MATLAB Function block to operate the respective relays as per the mode of operation.

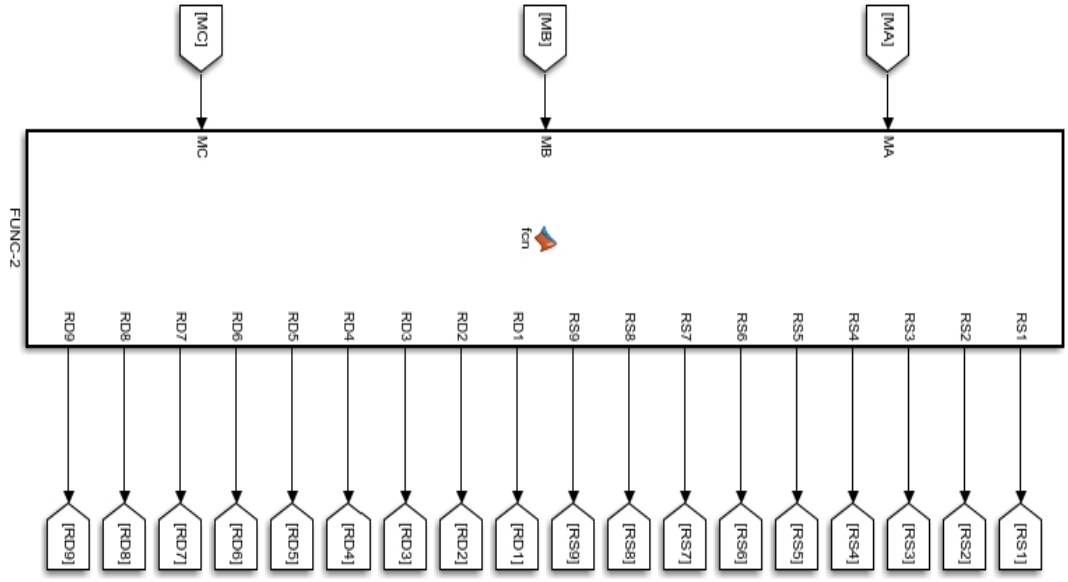


Figure 4.9: Function block to operate respective relay

4.4 Sub system (SUB-5) to switch respective IGBT

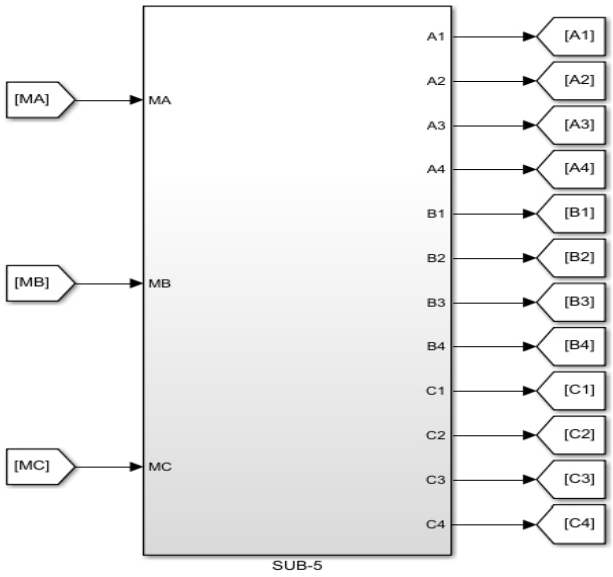


Figure 4.10: Sub system (SUB-5) to switch respective IGBT

Fig. 4.10 shows PWM generation subsystem for FT-CHBMLI. According to status of MA, MB and MC. Fig. 4.11 shows logic for PWM generation. State based switching has been utilized to generate gate pulses in different modes of operation.

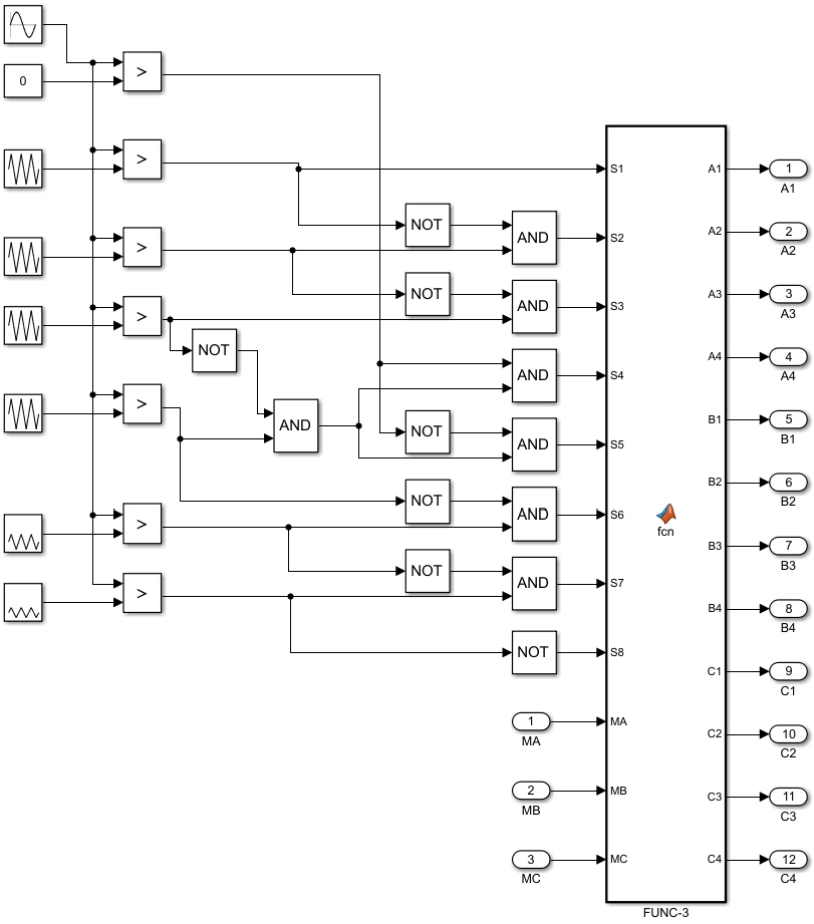


Figure 4.11 Sub system (SUB-5) logic circuit

4.5 Simulation Results

4.5.1 Mode-0: All modules healthy

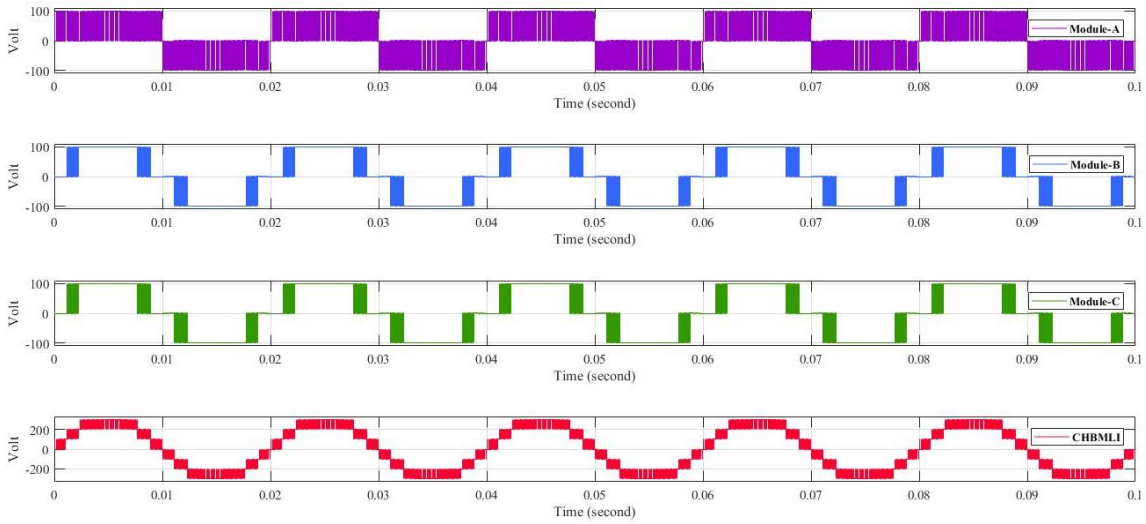


Figure 4.12 Output voltage waveforms under Mode-0

When all modules are healthy FT-CHBMLI operate under Mode-0 as shown in Fig. 4.12. Switching pattern of IGBTs under Mode-0 is shown in Table. 4.6. $V_a = V_b = V_c = 100$ V is used to simulate FT-CHBMLI. All three modules provide peak voltage of 100V. Combination of three modules provide 7-Level output voltage with peak voltage 300 V. As LS-PWM is utilized to generate PWM pulses, non-uniform power sharing among modules has been observed.

SWITCHING OF IGBT UNDER MODE-0

	Module-A (Healthy)				**Module-B** (Healthy)				**Module-C** (Healthy)				**Voltage**
State ↓	**A1**	**A2**	**A3**	**A4**	**B1**	**B2**	**B3**	**B4**	**C1**	**C2**	**C3**	**C4**	**Level**
S1	1	1	0	0	1	1	0	0	1	1	0	0	+3Vdc
S2	0	1	0	1	1	1	0	0	1	1	0	0	+2Vdc
S3	1	1	0	0	0	1	0	1	0	1	0	1	+Vdc
S4	0	1	0	1	0	1	0	1	0	1	0	1	0
S5	0	1	0	1	0	1	0	1	0	1	0	1	0
S6	0	0	1	1	0	1	0	1	0	1	0	1	-Vdc
S7	0	1	0	1	0	0	1	1	0	0	1	1	-2Vdc
S8	0	0	1	1	0	0	1	1	0	0	1	1	-3Vdc

Table 4.6: Switching of IGBT under Mode-0

4.5.2 Mode-0 to Mode-1 (Module-A Faulty)

When module A becomes faulty at 0.04s, two modules (B & C) remains in operating condition. RS1 and RD3 are operated to isolate Module-A. Output voltage of Module-A becomes zero as shown in Fig. 4.13 Only bypassing the first module and continuing with other two does not provide required output voltage magnitude. To maintain the output voltage RS2, RS3, RD1 and RD5 are operated, which connected source of Module-A in series with the source of Module-B which can be observed from Fig. 4.13. After fault occurrence at 0.04s, peak voltage of Module-B becomes 200V. To generate 7-Level output voltage using Module-B (200 V_{dc}) & Module-C (100 V_{dc}), Gate pulses should be modified as shown in Table. 4.7. 7-Level output voltage after fault condition is shown in Fig. 4.13.

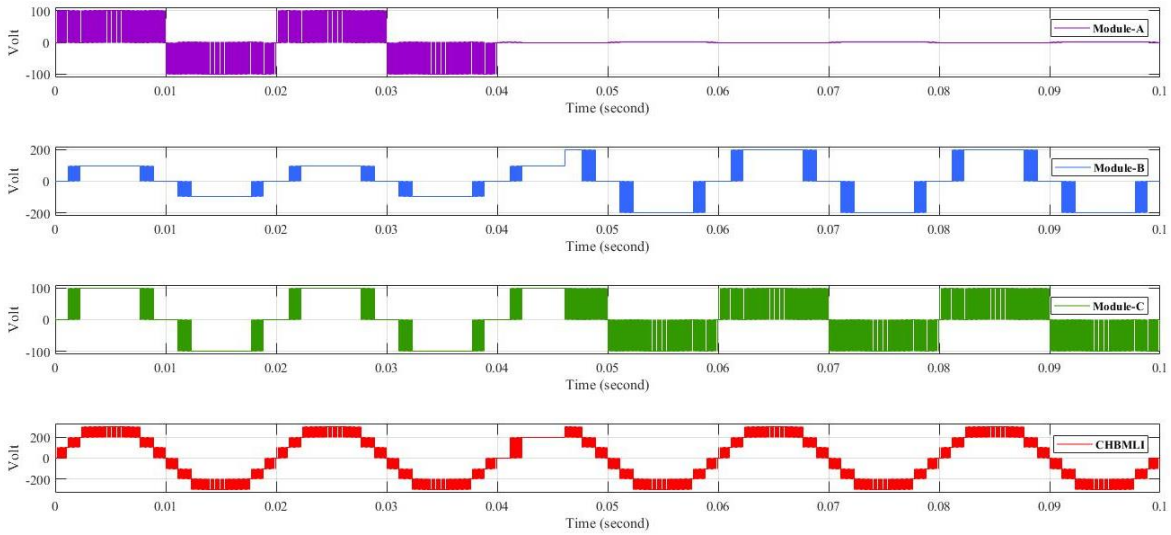


Figure 4.13: Output voltage waveforms under Mode-1

SWITCHING OF IGBT UNDER MODE-1

	Module-A (Faulty)				Module-B (Healthy)				Module-C (Healthy)				Voltage Level
State ↓	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	
S1	0	0	0	0	1	1	0	0	1	1	0	0	+3Vdc
S2	0	0	0	0	1	1	0	0	0	1	0	1	+2Vdc
S3	0	0	0	0	0	1	0	1	1	1	0	0	+Vdc
S4	0	0	0	0	0	1	0	1	0	1	0	1	0
S5	0	0	0	0	0	1	0	1	0	1	0	1	0
S6	0	0	0	0	0	1	0	1	0	0	1	1	-Vdc
S7	0	0	0	0	0	0	1	1	1	0	1	0	-2Vdc
S8	0	0	0	0	0	0	1	1	0	0	1	1	-3Vdc

Table 4.7: Switching of IGBT under Mode-1

4.5.3 Mode-0 to Mode-2 (Module-B Faulty)

When Module-B becomes faulty at 0.04s, two modules (A & C) remains in operating condition. RS2 and RD6 are operated to isolate Module-B and output of Module-B becomes zero at 0.04s as shown in Fig. 4.14. To maintain the output voltage magnitude same as in healthy condition RS3, RS5, RD4 and RD8 are operated, which connected source of Module-B in series with the source of Module-C and output of Module-C increases. To generate 7-Level output voltage using Module-C (200 V_{dc}) & Module-A (100 V_{dc}), Gate pulses should be modified as shown in Table. 4.8. 7-Level output voltage can be observed after the fault occurrence with same voltage magnitude as in healthy condition.

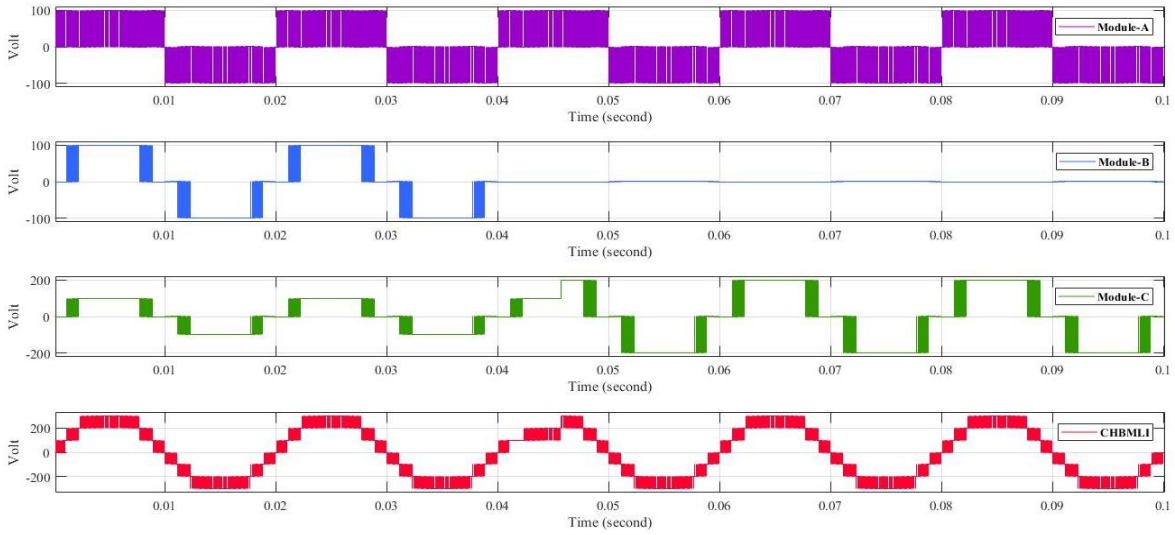


Figure 4.14 Output voltage waveforms under Mode-2

SWITCHING OF IGBT UNDER MODE-2

	Module-A (Healthy)				Module-B (Faulty)				Module-C (Healthy)				Voltage Level
State ↓	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	
S1	1	1	0	0	0	0	0	0	1	1	0	0	+3Vdc
S2	1	0	1	0	0	0	0	0	1	1	0	0	+2Vdc
S3	1	1	0	0	0	0	0	0	1	0	1	0	+Vdc
S4	0	1	0	1	0	0	0	0	1	0	1	0	0
S5	0	1	0	1	0	0	0	0	1	0	1	0	0
S6	0	0	1	1	0	0	0	0	1	0	1	0	-Vdc
S7	1	0	1	0	0	0	0	0	0	0	1	1	-2Vdc
S8	0	0	1	1	0	0	0	0	0	0	1	1	-3Vdc

Table 4.8: Switching of IGBT Under Mode-2

4.5.4 Mode-0 to Mode-3 (Module-C Faulty)

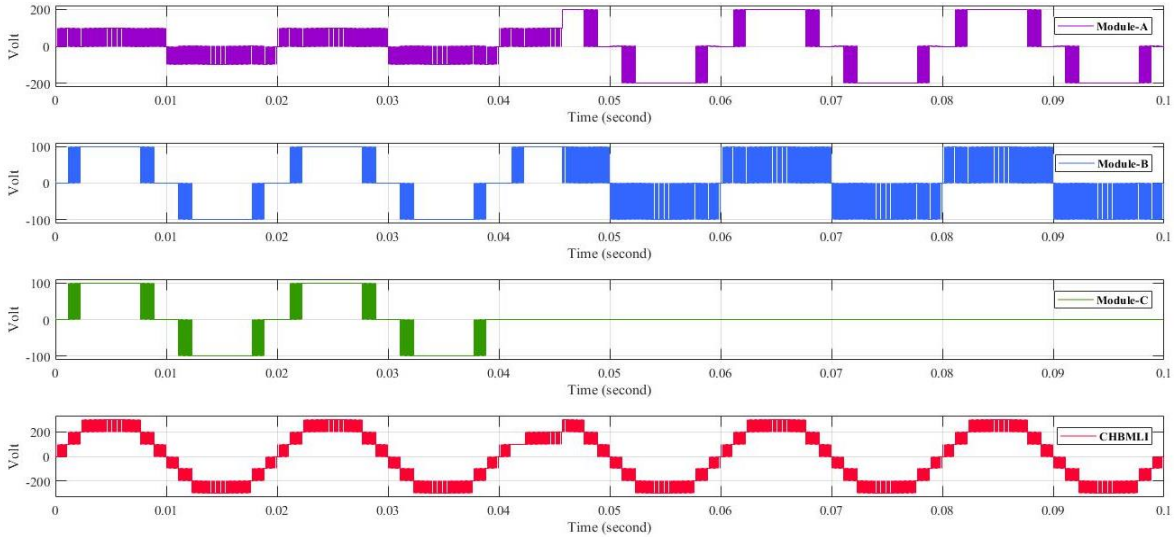


Figure 4.15: Output voltage waveforms under Mode-3

When Module-C becomes faulty at 0.04s, two modules (A & B) remains in operating condition. RS6, RD7 and RD8 are operated to isolate Module-C and its output reduces to zero as shown in Fig. 4.15. To maintain the output voltage magnitude same as in healthy condition RS7, RD1 and RD9 are operated, which connected source of Module-C in series with the source of Module-A. Module-A operate with 200 V DC as input. To generate 7-Level output voltage using Module-A (200 V_{dc}) & Module-B (100 V_{dc}), Gate pulses should be modified as shown in Table. 4.9.

SWITCHING OF IGBT UNDER MODE-3

	Module-A (Healthy)				Module-B (Healthy)				Module-C (Faulty)				Voltage Level
State ↓	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	
S1	1	1	0	0	1	1	0	0	0	0	0	0	+3Vdc
S2	1	1	0	0	1	0	1	0	0	0	0	0	+2Vdc
S3	1	0	1	0	1	1	0	0	0	0	0	0	+Vdc
S4	0	1	0	1	0	1	0	1	0	0	0	0	0
S5	0	1	0	1	0	1	0	1	0	0	0	0	0
S6	0	1	0	1	0	0	1	1	0	0	0	0	-Vdc
S7	0	0	1	1	0	1	0	1	0	0	0	0	-2Vdc
S8	0	0	1	1	0	0	1	1	0	0	0	0	-3Vdc

Table 4.9: Switching of IGBT under Mode-3

4.5.5 Mode-0 to Mode-4 (Module-A & Module-B Faulty)

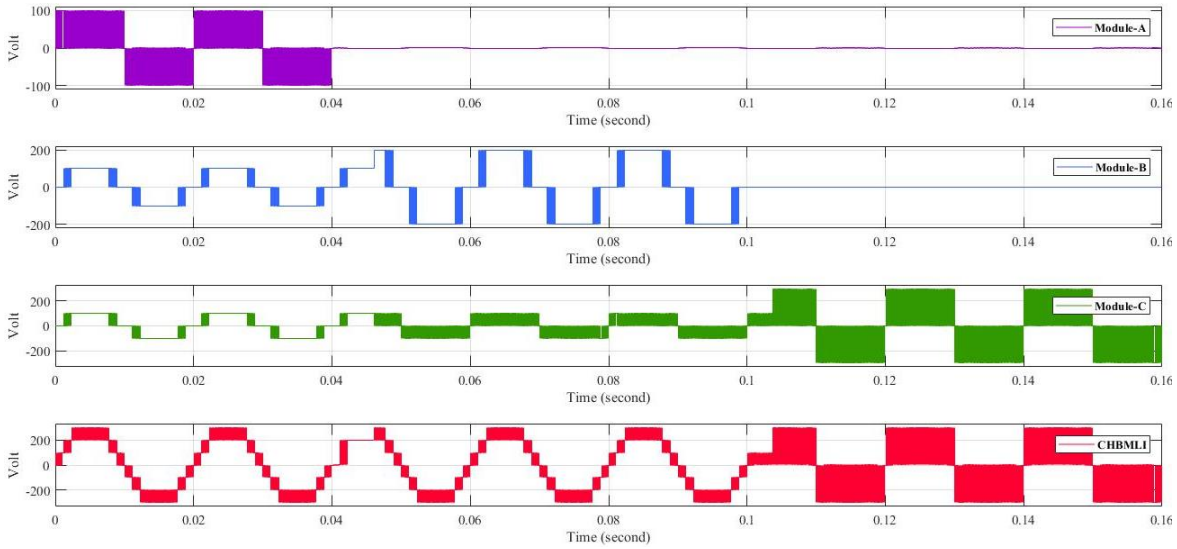


Figure 4.16: Output voltage waveforms under Mode-4

Fig. 4.16 shows the transition from Mode-0 to Mode-1 (at 0.04s) and Mode-1 to Mode-4(at 0.1s). At 0.04s Module-B becomes faulty & at 0.1s Module-A becomes faulty. After 0.1s, only Module-C remains in operating condition. When the first fault

occurred in Module-A, it gets isolated by respective relays. Further occurrence of second fault in Module-B, operate RS4, RD5 and RD6 to isolate Module-B. As the module is faulty and get isolated, output voltage of Module-B becomes zero at 0.1s. To maintain the output voltage magnitude same as in healthy condition sources of Module-A and Module-B utilized along with the source of Module-C. RD1 are operated to connect source of Module-A to Module-C.RS2 and RS5 are operated to connect voltage sources of Module-C and Module-B in series with Module-A. Series connection of all three sources provide $3V_{dc}$ input voltage to Module-C which can be observed from the output voltage of Module-C in Fig. 4.16. To generate 3-Level output voltage using Module-C (300 V_{dc}). Gate pulses should be modified as shown in Table. 4.10.

SWITCHING OF IGBT UNDER MODE-4

	Module-A (Faulty)				Module-B (Faulty)				Module-C (Healthy)				Voltage Level
State ↓	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	
S1	0	0	0	0	0	0	0	0	0	0	0	0	0
S2	0	0	0	0	0	0	0	0	0	0	0	0	0
S3	0	0	0	0	0	0	0	0	1	1	0	0	+3Vdc
S4	0	0	0	0	0	0	0	0	1	0	1	0	0
S5	0	0	0	0	0	0	0	0	0	1	0	1	0
S6	0	0	0	0	0	0	0	0	0	0	1	1	-3Vdc
S7	0	0	0	0	0	0	0	0	0	0	0	0	0
S8	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4.10: Switching of IGBT Under Mode-4

4.5.6 Mode-0 to Mode-5 (Module-B & Module-C Faulty)

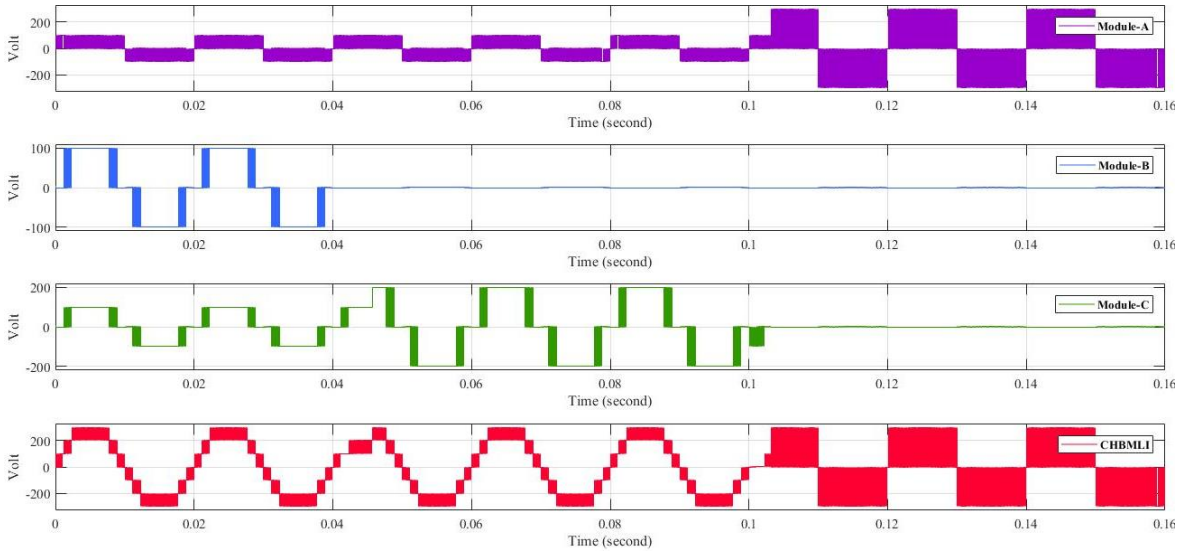


Figure 4.17: Output voltage waveforms under Mode-5

Fig. 4.17 shows the transition from Mode-0 to Mode-2 (at 0.04s) and Mode-2 to Mode-5(at 0.1s). At 0.1s, Module-B & Module-C both becomes faulty. After second fault in Module-C, only Module-A remains in operating condition. RS6, RD7, RD8 are operated Module-C at 0.1s reducing its output voltage to zero. To maintain the output voltage magnitude same as in healthy condition sources of Module-B and Module-C utilized along with the source of Module-A. RS3, RD4 and RD9 are operated to connect source of Module-B to Module-C. RS8 are operated to connect voltage sources of Module-A in series with Module-B. RS7 is operated to connect source of Module-C with Module-A. Series connection of all three sources provide $3V_{dc}$ input voltage to Module-A which can be verified from the output voltage of Module-A after 0.1s. To generate 3-Level output voltage using Module-C (300 V_{dc}). Gate pulses should be modified as shown in Table. 4.11.

SWITCHING OF IGBT UNDER MODE-5

	Module-A (Healthy)				Module-B (Faulty)				Module-C (Faulty)				Voltage Level
State ↓	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	
S1	0	0	0	0	0	0	0	0	0	0	0	0	0
S2	0	0	0	0	0	0	0	0	0	0	0	0	0
S3	1	1	0	0	0	0	0	0	0	0	0	0	+3Vdc
S4	1	0	1	0	0	0	0	0	0	0	0	0	0
S5	0	1	0	1	0	0	0	0	0	0	0	0	0
S6	0	0	1	1	0	0	0	0	0	0	0	0	-3Vdc
S7	0	0	0	0	0	0	0	0	0	0	0	0	0
S8	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4.11: Switching of IGBT Under Mode-5

4.5.7 Mode-0 to Mode-6 (Module-A & Module-C Faulty)

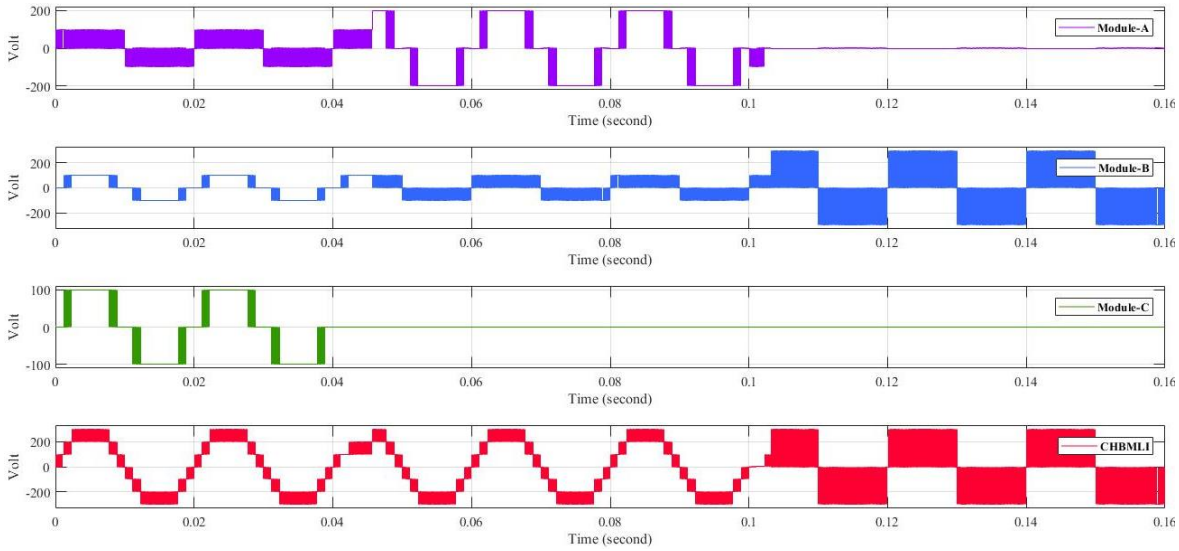


Figure 4.18 Output voltage waveforms under Mode-6

Fig. 4.18 shows the transition from Mode-0 to Mode-3 (at 0.04s) and Mode-3 to Mode-6(at 0.1s). When Module-A & Module-C becomes faulty, Module-B remains in operating condition. RS1, RD3 are operated to isolate Module-A at 0.1s as shown in Fig. 4.18. To maintain the output voltage magnitude same as in healthy condition sources of Module- A and Module-C utilized along with the source of Module-B. RD5 is utilized to isolate source of Module-B and RS2 is operated to connect it with source of Module-A. RD1 and RD9 are operated to connect source of Module-A with source of Module-C. Finally, RS9 connect source of Module-C to Module-B. Series connection of all three sources provide $3V_{dc}$ input voltage to Module-B. To generate 3-Level output voltage using Module-C ($3V_{dc}$). Gate pulses should be modified as shown in Table. 4.12.

SWITCHING OF IGBT UNDER MODE-6

	Module-A (Faulty)				Module-B (Healthy)				Module-C (Faulty)				Voltage Level
State ↓	A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	
S1	0	0	0	0	0	0	0	0	0	0	0	0	0
S2	0	0	0	0	0	0	0	0	0	0	0	0	0
S3	0	0	0	0	1	1	0	0	0	0	0	0	+3Vdc
S4	0	0	0	0	1	0	1	0	0	0	0	0	0
S5	0	0	0	0	0	1	0	1	0	0	0	0	0
S6	0	0	0	0	0	0	1	1	0	0	0	0	-3Vdc
S7	0	0	0	0	0	0	0	0	0	0	0	0	0
S8	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4.12: Switching of IGBT under Mode-6

4.5.8 Change in Modulation Index

LS-PWM shown in Fig. 4.19 is utilized to generate switching pulses for 7 level CHBMLI. LS-PWM has six triangular carrier and one sinusoidal reference. As the reference travels through carrier waveform it travels through 8 different sectors as defined in Table. 4.13.

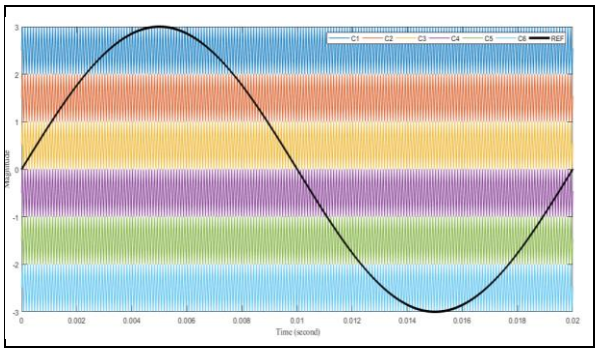


Figure 4.19 LS-PWM

Table 4.13 State selection for IGBT switching

Sr.	Condition	State	Voltage
1	REF > C1	S1	$3V_{dc}$
2	C1 ≥ REF > C2	S2	$2V_{dc}$
3	C2 ≥ REF > C3	S3	V_{dc}
4	C3 ≥ REF > 0	S4	0
5	0 ≥ REF > C4	S5	0
6	C4 ≥ REF > C5	S6	$-V_{dc}$
7	C5 ≥ REF > C6	S7	$-2V_{dc}$
8	REF ≤ C6	S8	$-3V_{dc}$

Each state represents different voltage level as shown in Table. 4.13. In seven level CHBMLI, there are three modules having same input voltage of V_{dc}. These modules are utilized in different state to get 7 different voltage magnitude during one cycle. Seven level of output is generated by means of series connection of three modules which are able to generate only 3 levels of output V_{dc}, $-V_{dc}$ and zero if operated individually. To get all 7 levels reference should travel along the eight sectors. This limitation restricts the modulation index up to 0.66. Below 0.66 modulation index, reference does not able to travel in S1 and S8, and one out of three modules does not get operated. Five level output can be generated by means of two modules as reference travels from S2 to S7. Result with 0.7 modulation index is shown in Fig. 4.20.

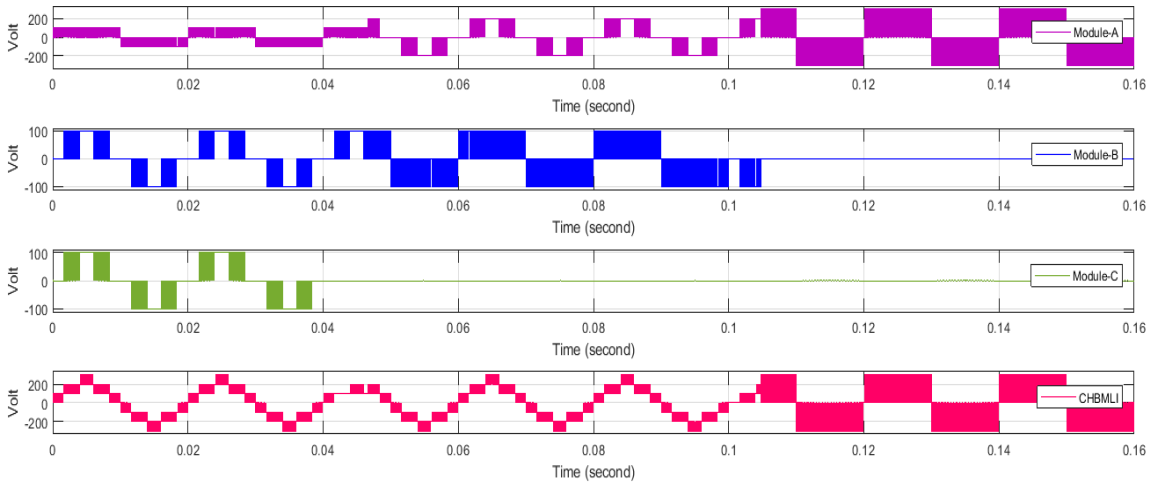


Figure 4.20: Output Voltage under Mode-5 (Modulation Index 0.7)