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DESIGN METHODOLOGIES FOR LOW POWER AND HIGH SPEED FULL ADDER

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Abstract
In this paper, different techniques involved in designing high performance with minimum power consuming full adder circuits are discussed and compared. Full adder plays an important role in portable digital applications such as PDAs, mobile phones, DSPs and address calculation for cache or memory accesses. It is one of the critical element in any digital communication device as there is a basic role of addition in all arithmetic circuits present in these electronic devices. However, as there is a limited amount of power available for the portable battery operated devices, the amount of power consumed by full adders is to be reduced and accordingly high performance is to be achieved.
Key words: Full Voltage Swing, Hybrid Adder, Power Delay Product, CMOS, FinFET, CNTFET

1. Introduction

Pervasive modern electronic systems are an integral part of day-today life. The demand for low power and high speed electronic systems is steadily increasing with the escalating applications in portable digital communication devices. Full adder is one of the basic building block in ALU, binary adder and multiplier, which are used in the devices such as mobile phones, digital calculators, smart watches, personal digital assistant etc. Adders are also the part of the critical path in most of the VLSI systems that determines the overall performance of the system. Therefore,it has become necessary to design efficient adder structures.In MOSFET based technology, miniaturization and optimization of transistor to nano-scale ranges has become the domineering parameter. With the reduction in chip-area, performance and power consumption of the adder cell is also affected. The power dissipation can be static power dissipation or dynamic power dissipation. Power dissipation due to gate leakage through gate dielectric, junction leakage from source/drain diffusion and sub-threshold leakage through off transistor can be termed as static dissipation. Whereas, dynamic power dissipation comprises of short-circuit power and switching power respectively. When both PMOS and NMOS stacks are partially ON , short-circuit current is present. When the switching of gate takes place, charging and discharging of load capacitances begins and hence switching power consumption comes into effect. Product of power and delay (PDP) is another key objective to be calculated for an efficient full adder design .Several hybrid design styles for designing efficient full adders are available which has low power consumption, improved performance, full output voltage swing and high output driving capability.

2. Literature survey

Based on Logic structure, full adder is of two types:- dynamic style and static style. Dynamic CMOS design has faster switching speed in comparison to static CMOS design. It has full swing voltage levels, no static power consumption and has less no. of transistor count. However, due to unwanted switching in idle mode, it has more power consumption and is more susceptible to leakage current. Therefore, dynamic CMOS designs for full adders is not suitable for battery operated systems. Apart from more on-chip area requirement, Static CMOS design styles are more reliable and has low power consumption comparing with dynamic style.
Depending upon the full output voltage swing and non full swing output voltage full adders can further be classified. The one bit full adder cell can be used as a elementary block for ripple carry adder, carry save adder, carry bypass adder, carry look ahead adder, carry skip adder and carry select adder. Different static CMOS design styles under full swing and non-full swing category are discussed. The different sub-category of static CMOS includes hybrid CMOS logic style[2], standard CMOS logic style[14], Complimentary Pass transistor Logic style (CPL)[14],Pass Transistor logic style(PTL)[14] ,Transmission Gate logic style(TG)[15], Static Energy Recovery Full adder(SERF) and Gate diffusion input(GDI) technique.

Conventional CMOS based full adder are designed which provides full swing output voltage with more transistor count. The complementary pass transistor logic(CPL) is a double rail architecture and is employed with cross-coupled PMOS transistors and output static inverters, due to which it provides better performance and full-

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swing output. Another type of full adder design style includes transmission function theory and transmission gates. Full adder using TG logic style has no issues of voltage loss. Therefore, they are used for designing XOR/XNOR gates .

Hybrid CMOS design style[3] is an another way to design low power and enhanced performance full adder. One of the way to design hybrid CMOS full adder can be using two or more modules including simultaneous XOR-XNOR gate or XOR/XNOR gate and a 2X1 multiplexer.

Apart from the conventional CMOS technology, other technologies such as FinFET, CNTFET, SET, GNRFET and QCA are also available which can be used for designing full adders with improved power delay product. It is seen that as the transistor is scaled down to the lower technology node, specifically beyond 28nm, FinFET technology provides lower power consumption and high speed in comparison to the CMOS technology.Also, if we compare CNFET technology with CMOS technology, CNFET cell has a low standby leakage current and improved performance.

In next Section ,out of the different technologies available, hybrid full adder circuits based on CMOS, FinFET and CNTFET technology are discussed.

Full Adder Logic Styles

1. Mariano Aguirre-Hernandez etal. [5]

An alternative internal logic system with pass-transistor logic styles(DPL and SR-CPL) has been used to design full-adder cells. The full adder cells exhibits reduced PDP. Thus, resulting in high performance and low power consumption.

In this methodology, multiplexer is used with input carry Cin as select line and A and B as input for the generation of Sum and Cout respectively. When input carry is zero, output is A xor B and when input carry is one, output is A xnor B. Using this design, the altogether propagation delay of full adder is reduced. Also ,the capacitive load for Cin is also reduced along with the improvement in performance for load sensitive application is also achieved. The proposed design is efficient enough to provide better power delay product (PDP).

Block diagram for Aguirre's Circuit is as follows:-

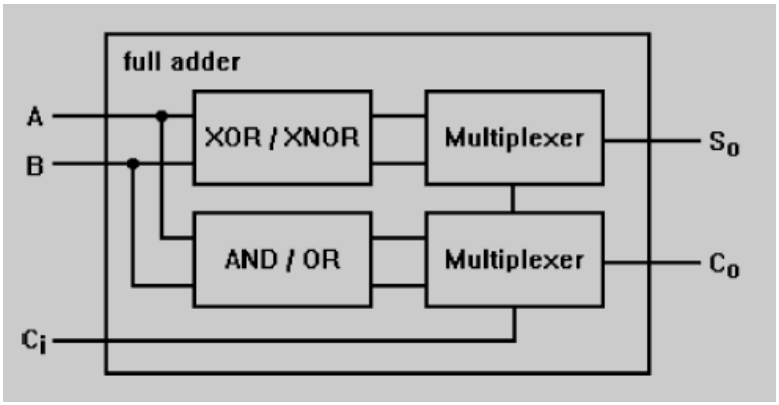

Fig.1:-Aguirre's Circuit

The proposed design is simulated at 180nm CMOS technology, 1.8V voltage and 200 MHz frequency.

2.Vahid Foroutan etal [6]

Two hybrid CMOS full adder logic style are discussed in this paper. One of the design is based on semi XOR/XNOR circuit and the other is based on GDI technique. A new Carry output circuit is designed. As ,the designing of xor-xnor circuit is quite composite , GDI technique is proposed.

Gate diffusion input(GDI) technique is a ultralow power, improved performance methodology for designing full adder cell. Therefore, the proposed technique uses GDI cell with ultra low power diode to eliminate the leakage current and to improve the output driving capability. This technique helps in reduction of static power and dynamic power. However, full adder based on GDI suffers from output driving capability, when cascaded. The proposed adder is simulated at 90nm and 180nm technology at an operating frequency of 100MHz. For 90nm technology, the supply voltage range is 0.8V to 1.4V and for 180nm technology, it is ranging from 0.6V to 1.2V.

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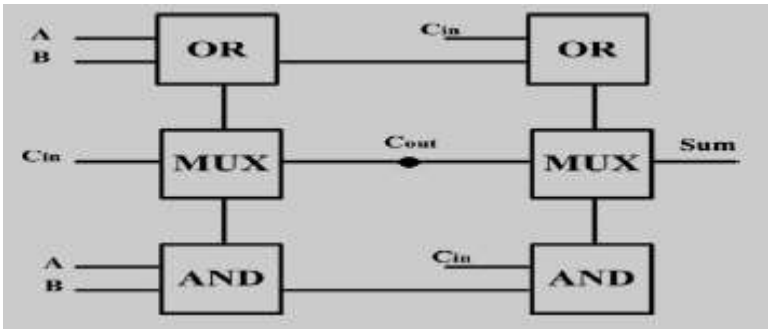

Fig.2:- Logic circuit for designing full adder cell

3.Mohan Shoba etal [7]

Three different designs for full adders are proposed, with full swing XOR, OR and AND logic gates , which helps in reducing threshold voltage problem. With the proposed methodology, output driving capability for cascaded operation is improved which also favors for faster operation. The proposed full adder is simulated at 45nm technology with 1.1V power supply and 100MHz operating frequency.

4. Parth Bhattacharya etal[8]

In this design approach, one bit hybrid full adder is designed using TG logic and CMOS logic. There are three blocks in this design. The first two blocks are the modified XNOR circuits that generates the SUM output and the third block is used to generate Cout signal. The XNOR module consumes more power in the full adder cell.

Therefore, to reduce power, incorporation of weak inverters in XNOR circuit (channel width of transistor being very small) is done whereas, the propagation delay of the carry signal is reduced by the intentional use of transmission gate whose channel width is made large for some of the transistor used in design. The proposed full adder cell is designed using 16 transistor. However, as the output driving capability is not strong enough, buffers are inserted at appropriate adder stages , when used in chain structure such as 32bit adder structure.

Block diagram below shows the proposed full adder cell.

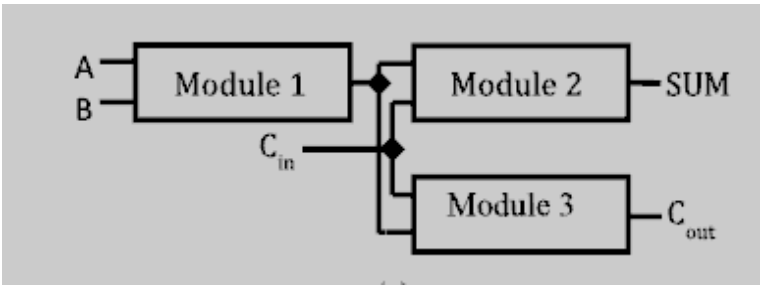

Fig..3:- Bhattacharya Circuit

The proposed adder is simulated using 180nm and 90nm technology and supply voltage of 1.2V and 1.8V respectively.

5.Pankaj Kumar etal [9]

The one bit full adder cell is constructed in such a way that it provides low voltage and high performance, resulting in an improved PDP. The slight modifications done internally results in a full output voltage swing with no additional delay. The input signal carry signal, which is not generated internally, commands the output signal sum and carry output. The proposed technique provides good output driving capability for the load connected to it. The proposed design is cost effective also due to the modification in the internal logic structure ,designed with input carry signal C and which consists of XOR/XNOR gates, modified NOR and NAND gates with multiplexers inserted at the output. Selection of the sum and carry outputs is done with the help of multiplexers. Full output voltage swing at low voltages is obtained with the proposed design.

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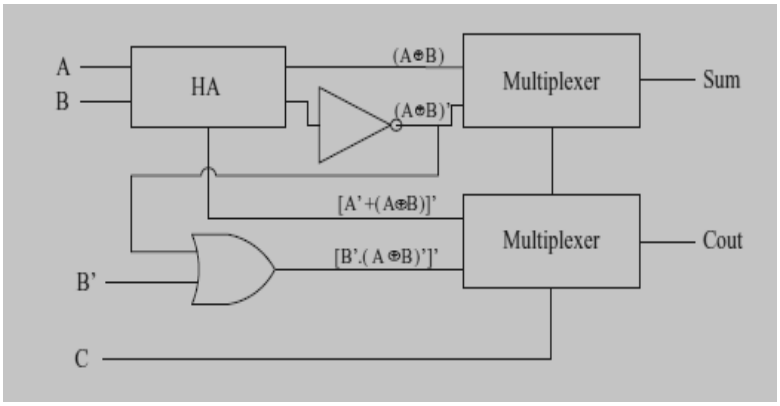

Fig. 4:-Proposed Architecture

When Cin = 0
Sum output = (A ⊕B),carry output = [A'+ (A ⊕B)]'
When Cin=1
Sum output = (A ⊕B)' , carry output = [B '.(A ⊕B)']

The proposed full adder is simulated at 55nm nd 90nm CMOS technology with a voltage extending from 0.4V - 1.2V and operating frequency of 100Mhz.

Reduction in output driving capability and large short circuit current are some of the limitations of the proposed technique.

6. Hamed Naseri etal [10]

One of the fundamental block for designing full adder is xor and xnor circuit, therefore, authors have proposed novel circuits for xor/xnor function or simultaneous xor-xnor function, which are optimized in terms of power consumption and delay, by using particle swarm optimization algorithm, which is to select the appropriate size of transistor. The proposed xor and xnor functions are used to design six types of full adders based on different applications. Proposed xor /xnor circuit is designed using 10 transistor and the proposed simultaneous xor-xnor circuit is designed using 12 transistor count. Simulation result shows that the proposed circuit has very good performance in different conditions.

The proposed full adders are simulated at 65nm CMOS technology with a voltage ranging from 0.8V-1.2V and operating frequency of 1GHz.

7. Majid Amini-Valashani etal [11]

Novel full swing, low power and energy efficient one bit 18 transistor in count full adder is designed using proposed 10 transistor XOR-XNOR cell .The XOR-XNOR cell is combined with a feedback loop and consists of modified pass transistor based 3 transistor XOR-XNOR gates and inverter.

The first block is implemented using the XOR-XNOR circuit, which is designed to reduce energy and power delay product of the complete adder and provides the output and its complement which is used as an input for the next two blocks. The circuits of the second and third block are designed in such a way that it provides less threshold voltage loss at the output node. In the proposed full adder, the sum and carry are outputs, generated separately and which also results in full voltage swing output.

The proposed full adder is simulated using 180nm technology with 1.8V power supply and 100Mhz operating frequency.

8.Mewada et al [12]

The performance of hybrid CMOS full adder cell and adder based on transmission gate logic style used in chain structures, can be improved without the use of buffers with a new design approach known as “triplet design”. This design is specifically meant for long chain structures.

In a "triplet design", breaking of propagation in the carry circuit of chain arrangement was done which helps in reducing the input carry load.In a “triplet design”, three FA topologies were used to construct the chain and cascade arrangement without the use of buffers.

The TG based and hybrid CMOS based full adder design can be converted to triplet design by satisfying the two conditions. The first condition is that the full adder design must includes both Cin and its complement signal. The second condition is that the Cout or its complement was generated from the transmission gate type multiplexers.

With this, two new hybrid CMOS full adders are designed. These full adder designs are used to build ripple carry adder and multipliers with decreased PDP.

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The proposed triplet design is simulated using gdpk045 library with 1V power supply and an operating frequency ranging from 25Mhz-200Mhz. This design does not provide better PDP for short chain structures and also thorough characterization of triplet design for all input test pattern is not done.

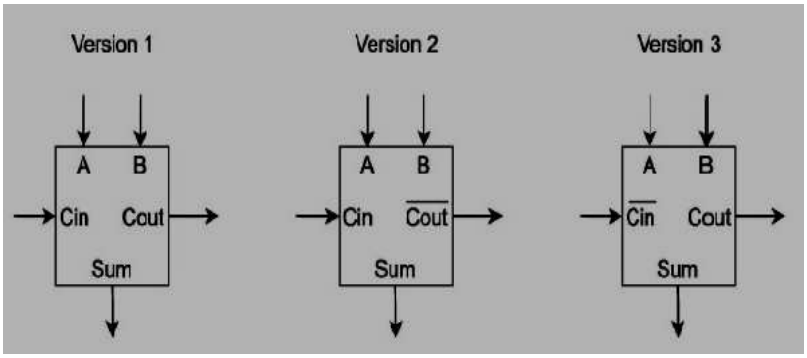

Fig.5:- Proposed triplet design of full adder

9. Saraswat etal [17]

A one bit full adder cell using 10 transistor count is designed using double gate FINFET (DG-FINFET) at 45nm CMOS technology node. The proposed design is simulated at 0.7V power supply. It is seen from the results that leakage current and leakage power is largely reduced to 25-30% as compared to CMOS adder cell with a trade-off of marginal increase in area.

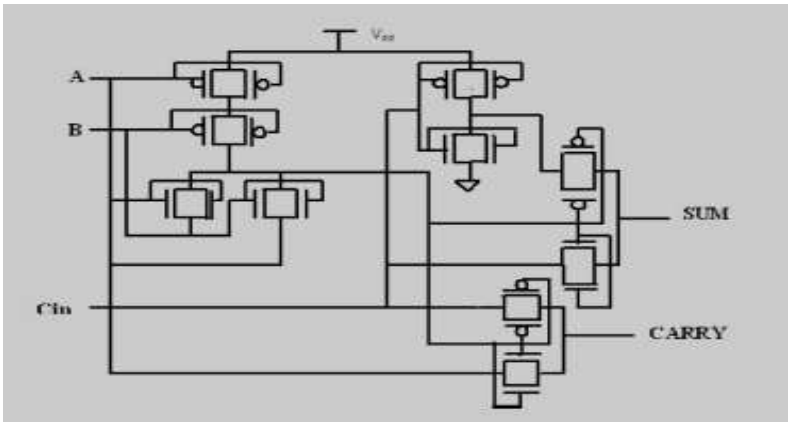

Fig.6:- Schematic design of one bit full adder cell using FINFET technology

10. Aqilah binti Abdul Tahrim etal.[18]

Different cell designs such as CMOS, CPL, TG and HCMOS are implemented using FINFET technology for designing one bit full adder operating in sub threshold region. Simulation were done at 16nm technology using HSPICE so as to measure performance(PDP) and energy efficiency (EDP)of the cells.

Out of the different cells, simulation results shows that one bit CPL FINFET based full adder has low power delay product(PDP) and improved energy efficiency(EDP).One of the reason for the improved PDP is that the CPL cell provides full swing operation with high speed.

The obtained results also shows that as the FinFET structure has multiple gates and can drive more current, it has faster switching speed than the MOSFET structure. Therefore, the adders based on FinFET technology has better performance.

11. Yavar Safaei Mehrabani et al.[19]

Two input XOR/XNOR cell are designed which are further used in designing one bit full adder cell using CNTFET technology. Five different XOR/XNOR cells are designed using collegial combination of Pass Transistor and Transmission Gate.

The first structure of XOR/XNOR cell named as "X-Design1", is designed using PTL and consists of 12 transistors. However, this design suffers from threshold loss problem when the input pattern is 00 and 11.This results in an increase in delay and power consumption.

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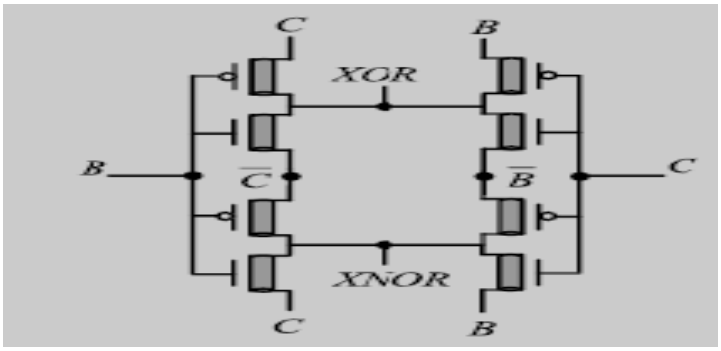

Fig.7: Proposed possible first design of XOR/XNOR cell

Therefore, in order to overcome this problem, the first design is modified using feedback loop and transmission gate technique. With this, another four structures are proposed , each having its own merits.

The second proposed design "X-Design2" of XOR/XNOR cell results in reduced short circuit power and delay, with a slight increase in an area overhead consisting of 14 transistors.

The third proposed design "X-Design3" of XOR/XNOR circuit has improved driving capability as compared to the first two designs with 18 transistors in count.

The fourth proposed XOR/XNOR design "X-Design4", has less transistor count but it suffers from reduced driving capability, whereas the last proposed design X-Design5 has less power consumption as compared to the fourth design.

The proposed XOR/XNOR circuits are further used to design five different types of full adder block. Simulations were done using HSPICE at 32nm Technology node.

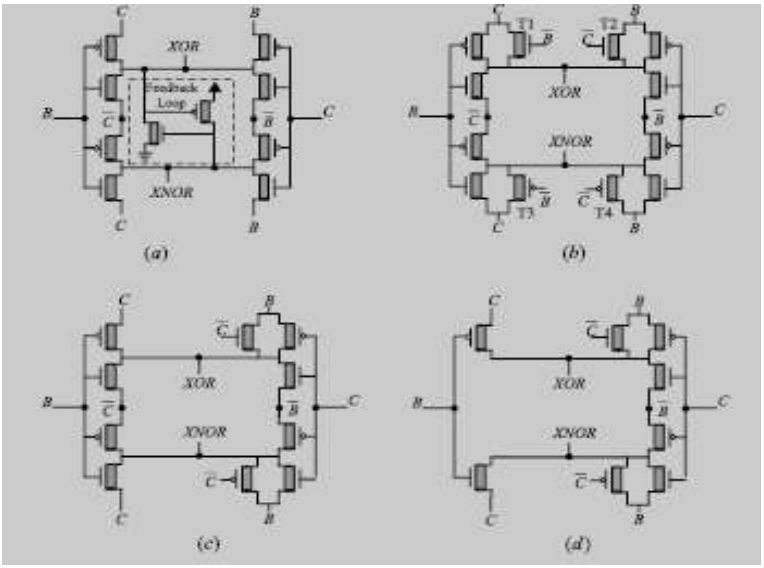

Fig.8 : Proposed XOR/XNOR cell (a) Second possible Design (b) Third possible Design (c) Fourth possible Design(d) Fifth possible Design

The comparison of the various technologies used for designing hybrid full adders can be better understood by the table shown below.

Table1:- Comparative Analysis of the proposed full adder design utilizing different technologies

Full Adder Designs	Technology Node	Supply Voltage	Freq.	PDP	Limitation
Paper1[5]	180 nm	1.8V	200Mhz	average PDP advantage of 80%,	Design is not capable of reducing power consumption and transistor. Count.
Paper2[6]	130nm, 90nm	0.8 to 1.4 V , 0.6 to 1.2V	100MHz	Approx.50% improvement with C-	Problems in the fabrication of Ultra Low Power Diode

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				CMOS	is taken into account.
Paper3 [7]	45nm	1.1V	100MHz	Power improvement -29.2% than conventional GDI based FA	Placing inverter on the critical path of the circuit results in an increased delay. More area overhead.
Paper4 [8]	180nm,90nm	1.2V/1.8V	-	20.5%-27.2% improvement in comparison to [20]	Not able to provide full output voltage swing at low supply voltages.
Paper 5[9]	180nm	1.8V	100MHz	35%–81% improvement	Presence of feedback results in an increase in delay and power consumption
Paper 6[10]	65nm	0.8V-1.2V	1 Ghz	16.2%–85.8%	Reduced output driving capability in chain str. application. Presence of NOT gate results in an increase delay.
Paper 7[11]	90nm,55nm	0.4V-1.2V	100MHz	44.73%-55nm, 76.69%-90nm improvement with C-CMOS	Output driving capability is not good, large short circuit current
Paper8[12]	gpdk 045 library	1V	25MHz-200MHz	Approx.25-50% reduction in PDP	Thorough characterization of triplet design for all input test patterns is not done. No better PDP obtained for short chain structure.
Paper 9[17]	45nm FinFET	0.7V	0.05GHz	25-30% reduction in power as compared to CMOS	Increased area overhead
Paper 10[18]	16nm FinFET	0.2V	-	Approx.50% reduction in PDP	Improved speed at the cost of increased power consumption.
Paper 11[19]	32nm CNTFET	0.8V- 1V	100MHz	Approx.50% -80% reduction in PDP	Presence of feedback – increased delay Lack of output driving capability.

3. Conclusion

Different types of hybrid full adder designs with less power consumption, enhanced performance, full swing output voltage, reduced area and low PDP with better driving capability were discussed in this paper. The design of full adder varies according to different applications. However, every adder design has its limitation also .It is generally seen that various adders based on CMOS technology, when used in chain structures has less output driving capability. In addition to this, if the inverter is placed on the critical path of the circuit, it results in an increase in delay. In order to increase the output voltage, the connected feedback loop results in an increased power consumption. Scaling in supply voltage results in degradation of performance.

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